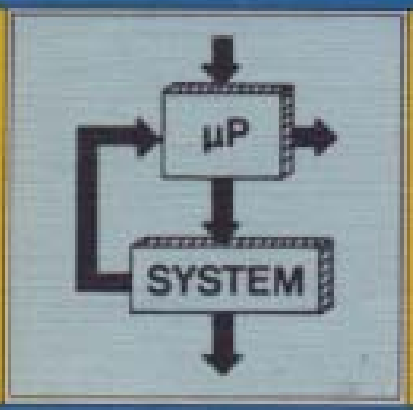
MULTI-MICROPROCESSOR SYSTEMS FOR REAL-TIME APPLICATIONS

EDITED BY

GIANNI CONTE

and

DANTE DEL CORSO



MICROPROCESSOR-BASED SYSTEMS ENGINEERING

D. REIDEL PUBLISHING COMPANY

DORDRECHT / BOSTON / LANCASTER

CONTENTS

PREFACE xi

1. MULTIPROCESSOR SYSTEM ARCHITECTURE 1
P. Civera, G. Conte and F. Gregoretti

1.1 DISTRIBUTED PROCESSING AND MULTIPROCESSORS 1
1.1.1 Classification Criteria 1
1.1.2 Computer Networks 2
1.1.3 Multiple Processor Systems 2
1.1.4 Special Purpose Machines 3
1.1.5 Other Classifications of Distributed Systems 4

1.2 MULTIPROCESSOR SYSTEMS 6
1.2.1 Multiprocessor Structures 6
1.2.2 The Interconnection Network 7
1.2.3 Shared Bus 8
1.2.4 Multiport Memory 9
1.2.5 Crossbar Switches 9
1.2.6 Multistage Interconnection Networks 11
1.2.7 Applications of Multiple Processors 12

1.3 DESCRIPTION TECHNIQUES FOR MULTIPROCESSORS 13
1.3.1 Levels of Description 13
1.3.2 Selection of the Description Level 14
1.3.3 The PMS Notation 15
1.3.4 The MSBI Notation 17

1.4 SOME MULTIPROCESSOR SYSTEMS 18
1.4.1 Selection Criteria 18
1.4.2 The Cm* 19
1.4.3 The C.mmp 20
1.4.4 The PLURIBUS 21
1.4.5 The μ^* System 23
1.4.6 The iAPX432 System 24
1.4.7 The TOMP Multiprocessor System 26

1.5 REFERENCES 30

2. PERFORMANCE ANALYSIS OF MULTIPROCESSOR SYSTEMS 33
M. Ajmone Marsan, G. Balbo and G. Conte.

2.1 PERFORMANCE EVALUATION OF BUS ORIENTED MULTIPROCESSOR SYSTEMS 33
2.1.1 Introduction 33
2.1.2 Modeling Assumptions 36
2.1.3 The System Workload 37
2.1.4 Architecture 1 41
2.1.5 Architecture 2 42
2.1.6 Architecture 3 48
2.1.7 Architecture 4 50
2.1.8 Architecture Comparison 53
2.1.9 Choice of the Architecure of TOMP 61

2.2 OTHER MODELING TECHNIQUES AND MEASUREMENTS 61
2.2.1 Introduction 61
2.2.2 Stochastic Petri Net Models 62
2.2.3 Queueing Network Models 69
2.2.4 Measurements 76

2.3 REFERENCES 82

3. TOMP SOFTWARE 87
F. Gregoretti

3.1 INTRODUCTION 87
3.1.1 Goals and Motivations 89
3.1.2 Limits 90
3.1.3 Overall System Description 90

3.2 INTERPROCESS COMMUNICATION 93
3.2.1 Model and Primitive Operations 93
3.2.2 Low Level Communication Protocol 98

3.3 THE EXECUTIVE 101
3.3.1 System Initialization 101
3.3.2 Process Management 102
3.3.3 Interrupt Handling 103
3.3.4 Monitoring Functions 105

CONTENTS

3.4 MONITORING AND DEBUG 106
3.4.1 General Architecture 106
3.4.2 Debugging Functions 108

3.5 UTILITIES 109
3.5.1 Terminal Handler 110
3.5.2 File System 110
3.5.3 Common Memory Allocator 111

3.6 SYSTEM GENERATION 112

3.7 A CRITICAL REVIEW 114

3.8 REFERENCES 115

4. DESIGN OF MULTIPROCESSOR BUSES 117
D. Del Corso

4.1 INTRODUCTION 117

4.2 BASIC PROTOCOLS 119
4.2.1 Elementary Operations 119
4.2.2 Types of Information Transfer Cycles 123
4.2.3 Synchronization of the Action Flow 129

4.3 BUSED SYSTEMS 133
4.3.1 Channel Allocation Techniques 133
4.3.2 Bus Arbitration 135
4.3.3 The Distributed Self-selection Arbiter 138

4.4 ELECTRICAL BEHAVIOUR OF BACKPLANE LINES 143
4.4.1 Definition of Signal Levels 143
4.4.2 Transmission Line Effects 145
4.4.3 Crosstalk 148
4.4.4 Protocol Speed 151

4.5 PROTOCOL EXTENSION 153
4.5.1 The Enable/Disable Technique 153
4.5.2 Bus Supervisors 157

4.6 REFERENCES 161

5. SOME EXAMPLES OF MULTIPROCESSOR BUSES 165
P. Civera, D. Del Corso and F. Maddaleno

5.1 INTRODUCTION 165

5.2 THE MULTIBUS BACKPLANE 166
5.2.1 History and Main Features 166
5.2.2 Physical and Electrical Specifications 166
5.2.3 The Information Transfer Protocol 170
5.2.4 Special Features 175
5.2.5 Timing and Pinout 178

5.3 THE VME BACKPLANE BUS 180
5.3.1 History and Main Features 180
5.3.2 Physical and Electrical Specifications 180
5.3.3 The Information Transfer Protocol 182
5.3.4 Special Features 185

5.4 THE 896 BACKPLANE BUS 188
5.4.1 History and Main Features 188
5.4.2 Physical and Electrical Specifications 188
5.4.3 The Information Transfer Protocol 191
5.4.4 Special Features 195
5.4.5 Timing and Pinout 196

5.5 THE M3BUS BACKPLANE 199
5.5.1 History and Main Features 199
5.5.2 Physical and Electrical Specifications 199
5.5.3 System Organization and Control 202
5.5.4 The Arbitration Protocol 203
5.5.5 The Addressing Protocol 206
5.5.6 The Data Transfer Protocol 208
5.5.7 Interrupt and Interprocessor Communication 213
5.5.8 Supervisor Protocol 215
5.5.9 The Serial Bus 219
5.5.10 Timing and Pinout 221

5.6 REFERENCES 223

CONTENTS

6. HARDWARE MODULES FOR MULTIPROCESSOR SYSTEMS 225
D. Del Corso and M. Zamboni

6.1 INTRODUCTION 225

6.2 SYSTEM DESIGN 226
6.2.1 Physical Organization of Multiprocessor Systems 226
6.2.2 Board Design Guidelines 229

6.3 SLAVE MODULES 231
6.3.1 Organization of Slave Modules 231
6.3.2 Address Decoders and Latches 233
6.3.3 Slave Control Logic 238
6.3.4 Slave Buffering 240

6.4 MASTER MODULES 241
6.4.1 Organization of Master Modules 241
6.4.2 External Access Decoder and Bus Arbitration 244
6.4.3 Master Control Logic 246
6.4.4 Master Buffering 248

6.5 INTERRUPT STRUCTURES 253
6.5.1 Requirements for Multiprocessor Systems 253
6.5.2 System Controls 254
6.5.3 Processor Interrupts 255
6.5.4 Centralized Interrupt Handler 256
6.5.5 Distributed Interrupt Handler 257
6.5.6 Serial Lines 261

6.6 SPECIAL MODULES 261
6.6.1 Multiple-slave Modules 261
6.6.2 Bus Windows 263
6.6.3 Dual-port Slaves 266
6.6.4 Master-slave Modules 270
6.6.5 Block Transfer Units 272
6.6.6 Supervisor Modules 273

6.7 REFERENCES 278

7. MULTIPROCESSOR BENCHMARKS 279
E. Pasero

7.1 INTRODUCTION 279

7.2 THE CONCEPT OF PERFORMANCE 280

7.3 PARALLEL PROGRAMMING 282

7.4 PARALLEL NOTATION FORM 283

7.5 PARALLEL SORTING TECHNIQUES 288

7.6 MEASUREMENTS AND ANALYSIS OF RESULTS 293

7.7 CONCLUSION 297

7.8 REFERENCES 298