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THESE DE DOCTORAT

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Development of control algorithms for renewable energy sources inverters in a microgrid environment

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Abstract

الملخص:

في الشبكات المصغرة المستقلة، من المهم الحفاظ على استقرار النظام وكذا تمكين مشاركة دقيقة للقدرة الفعالة والغير فعالة بين وحدات توليد الطاقة الموزعة المتصلة على التوازي. هذه الغاية هي مسؤولية المتحكم الأولي والذي يتكون من حلقات تحكم متعددة، وحدة حساب القدرة القائمة على التقدير، وحدة التحكم في التدلي (الانخفاض)، وحدة الممانعة الافتراضية، وحلقة التحكم في الجهد الداخلية. مع هذا، فإن مشكل ضعف مشاركة القدرة النشطة والقدرة الغير فعالة بسبب تأثيراختلاف الممانعة الخاصة بمغذيات وحدات التوليد الموزعة أمر حتمي عند اعتماد وحدات المراقبة التقليدية المدمجة في طبقة المتحكم الأولي. بالاضافة الى هذا، قد يؤثر وجود الأحمال غير الخطية وغير المتوازنة بشدة على دقة مشاركة القدرة الغير فعالة عند التحكم في الطاقة الفعالة، ومن الصعب مشاركة توافقيات التيار الخاصة بالحمل باستخدام هذه الوحدت التقليدية. لذلك، يعد تصميم أنظمة تحكم محسنة، المكونة للتحكم الأولي، أمرًا ضروريًا من أجل تحسين أداء الشبكات المصغرة من حيث دقة مشاركة الطاقة وكذا الاستقرار والمتانة لتحمل مختلف الاضطرابات. في هذا الصدد، الأطروحة المقدمة تهدف الى تطوير استراتيجيات تحكم متقدمة والتي تندرج تحت المتحكم الأولي وكذا توفير تحليل رياضي مفصل. أهم المساهمات المدرجة في هذه الأطروحة والخاصة بالمتحكم الأولي المخصص للشبكات المصغرة المستقلة أحادية الطور هي كالآتي:

- **تم اقتراح تصميم محسّن لـ SOGI-FLL، سمي ESOGI-FLL، مع إمكانية ازالة العنصر المستمر DC بهدف تقديم استخراج دقيق للمعلمات المفتاحية الخاصة بالجهد في الأنظمة أحادية الطور.**
- **تم تصميم مخطط لمتحكم الجهد الداخلي ذو الحلقة المزدوجة بإدراج مراقب من نوع نسبي-تكاملي (PI) مع استراتيجية التغذية الاسترجاعية في حلقة متحكم الجهد ومراقب نسبي (P) في حلقة التحكم في التيار.**
- **تم اقتراح مخطط تحكم محسن الخاصة بتشارك الطاقة يشتمل على وحدة مطورة لحساب القدرة وكذا حلقة مقاومة افتراضية متكيفة مع التردد .**

تؤكد النتائج التي تم الحصول عليها من خلال المحاكاة والاختبارات التجريبية فعالية وصلابة مخططات التحكم المقترحة في ضمان استقرار الشبكات المصغرة المستقلة وكذلك تشارك دقيق للطاقة بين وحدات الموزعة أحادية الطور المربوطة على التوازي حتى في ظل وجود أحمال غير الخطية.

Abstract:

In the islanded microgrids (MGs), it is important to maintain system stability and achieve proper active and reactive power-sharing between the parallel-connected distributed generation (DG) units. This objective is the responsibility of the primary control (PC) which consists of multiple control loops: an estimation-based power calculation unit, a droop control loop, a virtual impedance loop, and an inner voltage control loop. However, the problem of poor active and reactive power sharing, due to the impact of the impedance mismatch of the DG units' feeders, is inevitable when adopting the conventional control loops-based PC scheme. Furthermore, the presence of nonlinear and unbalanced loads may severely affect the accuracy of the reactive power sharing when controlling the active power and it is difficult to share the load current harmonics only by using these conventional control schemes. Therefore, the design of advanced control schemes, included in the primary control, is imperative in order to improve the MG performance in terms of power-sharing accuracy, stability, and robustness against load disturbances. In this regard, the present thesis focuses on developing advanced control strategies that are involved in the PC as well as providing detailed mathematical analysis. The main contributions made in this thesis to the PC intended for single-phase islanded AC MG, are:

- **An enhanced SOGI-FLL scheme; called ESOGI-FLL; suitable for DC-offset rejection is proposed for the aim of ensuring proper estimation of the voltage key parameters in single-phase systems.**
- **A scheme of the double-loop inner control is designed. A Proportional-Integral (PI), with feedforward control strategy, is used in the voltage control loop and a Proportional (P) control is used in the current control loop.**
- **An improved power sharing control scheme, that includes an enhanced power calculation unit and a frequency-adaptive virtual impedance loop, is proposed.**

The obtained results through simulations and experimental tests demonstrate the effectiveness and the robustness of the proposed control schemes in achieving stable MG operation and accurate power-sharing among single-phase paralleled DG units even under nonlinear loads operating conditions.

Résumé:

Dans les micro-réseaux fonctionnant en mode isolé, il est important de maintenir la stabilité du système et d'atteindre un partage approprié de la puissance active et la puissance réactive entre les sources d'énergie distribuées et connectées en parallèle. Cet objectif, est confié à la commande primaire (primary control (PC)) qui se compose de plusieurs boucles de commande : une unité de calcul de puissance basée sur une unité d'estimation, une boucle de commande de statisme (droop control), une boucle d'impédance virtuelle et une boucle de commande de tension interne. Cependant, le problème de partage inapproprié de la puissance active et la puissance réactive, à cause de l'impact de la discordance d'impédance des lignes des sources distribuées, ne peut pas être évité en utilisant les méthodes classiques de commande. De plus, la présence de charges non linéaires et déséquilibrées peut gravement affecter la précision du partage de la puissance réactive lors du contrôle de la puissance active, ainsi il est difficile de partager les harmoniques du courant de charge uniquement en utilisant les méthodes conventionnelles de commande. Par conséquent, le développement de stratégies de contrôle avancées incluses dans la couche de commande primaire est impératif, afin d'améliorer les performances du micro-réseau en termes de précision de partage de puissance, de stabilité et de robustesse vis-àvis des perturbations de la charge. A cet égard, la présente thèse s'intéresse au développement de stratégies de commande avancées impliquées dans le PC ainsi que de fournir une analyse mathématique détaillée. Les principales contributions apportées, dans cette thèse, à la commande primaire destinée pour un micro-réseau AC monophasée isolé sont :

- **Une méthode SOGI-FLL améliorée, nommé ESOGI-FLL et appropriée au rejet de la composante continue DC, est proposée dans le but de parvenir à une estimation correcte des paramètres clés de la tension d'un système monophasé.**
- **Une méthode de commande de la tension interne à double boucle est développée. Un régulateur proportionnelle-intégrale (PI), basée sur la stratégie de commande par anticipation, est utilisé dans la boucle de commande de la tension, et un régulateur proportionnel (P) est utilisé dans la boucle de commande du courant.**
- **Une technique améliorée de la commande du partage de la puissance est proposée. Cette technique inclut une unité de calcul de la puissance optimisée et une boucle de commande d'impédance virtuelle adaptative en fréquence.**

Les résultats des simulations et des essais expérimentaux effectués montrent l'efficacité et la robustesse des stratégies de commande proposées. Elles permettent d'assurer, même en présence de charges non-linéaires, un fonctionnement stable du micro-réseau et un partage de puissance précis entre les unités distribuées monophasées et connectées en parallèle.

Keywords: Islanded Microgrid, Single-phase system, Droop control strategy, Parallel-connected VSIs, Primary control, SOGI-FLL, ESOGI-FLL, MSOGI-FLL, MESOGI, Small-signal modeling, Power sharing control, Tuning procedure.

Dedication

To my mother

To my father

To my brothers and sisters

To my advisor and co-advisor for their support.

To all my friends.

Publications

Journal's Paper

- **A. Kherbachi,** A. Chouder, A. Bendib, K. Kara, S. Barkat, "*Enhanced structure of second-order generalized integrator frequency-locked loop suitable for DC-offset rejection in single-phase systems*," ***Electric Power Systems Research***, vol. 170, pp. 348-357, May 2019.

- Bendib, K. Kara, A. Chouder, **A. Kherbachi**, S. Barkat, "*New modeling approach of secondary control layer for autonomous single-phase microgrids*," ***Journal of the Franklin Institute***, vol. 356, no. 13, pp. 6842-6874, September 2019.

Conferences' Papers

- **A. Kherbachi,** A. Bendib, K. Kara and A. Chouder, "*ARM-based implementation of SOGI-FLL method for power calculation in single-phase power system*," ***2017 5th International Conference on Electrical Engineering - Boumerdes (ICEE-B)***, Boumerdes, 2017, pp. 1-6.

- A. Bendib, **A. Kherbachi**, K. Kara and A. Chouder, "*Droop controller-based primary control scheme for parallel-connected single-phase inverters in islanded AC microgrid*," ***2017 5th International Conference on Electrical Engineering - Boumerdes (ICEE-B),*** Boumerdes, 2017, pp. 1-6.

- **A. Kherbachi,** A. Chouder, A. Bendib, K. Kara, S. Barkat, "*Experimental Implementation of Droop Control Strategy for Single-Phase Parallel-Connected VSIs Forming Islanded AC Microgrid*," ***2018 International Conference on Electrical Sciences and Technologies in Maghreb (CISTEM)***, Algiers, 2018, pp. 1-6.

- Bendib, A. Chouder, K. Kara, **A. Kherbachi,** and S. Barkat, "*SOGI-FLL Based Optimal Current Control Scheme for Single-Phase Grid-Connected Photovoltaic VSIs with LCL Filter*," ***2018 International Conference on Electrical Sciences and Technologies in Maghreb (CISTEM)***, Algiers, 2018, pp. 1-6.

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List of Abbreviations and Symbols

PCC	Point of Common Coupling
RES	Renewable Energy Sources
DG	Distributed Generation
PV	Photovoltaic
ESS	Energy Storage System
VIL	Virtual Impedance Loop
MG	Microgrid
ESOGI	Enhanced Second-Order Generalized Integrator
FLL	Frequency Locked Loop
MSOGI	Multiple Second-Order Generalized Integrator
PC	Primary Control
PWM	Pulse Width Modulation
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
AC	Alternative Current
DC	Direct Current
DERs	Distributed Energy Sources
PID	Proportional-Integral Derivative
PLL	Phase Locked Loop
LPF	Low-Pass Filter
P	DG unit active power
Q	DG unit Reactive power
v_{MG}	MG voltage
v_g	Grid voltage
f_{MG}	MG frequency
E_{MG}	MG voltage Amplitude
f_{MG}	DG unit frequency
E_{MG}	DG unit voltage amplitude
v_o	Inverter Output voltage
i_o	Inverter output current
S	Complex power
P_g	MG active power
Q_g	MG reactive power

Chapter I:

Introduction to Microgrid Power Sharing Control

Chapter I:

Introduction to Microgrid Power Sharing Control

1.1 Background and Motivations

In the last years, humanity witnessed a technological development at rates never experienced before. Among the consequences, can be computed an unexpected increase in the energy demand over the years and the reduction of fossil fuels due to their massive deployment and finite availability [1–3]. The former is becoming an intolerable burden on the transmission network, while the latter, together with the awareness of the harmful effects of fossil fuels burning both on humans and the environment [4], [5], has brought to the spreading of renewable energy sources. Investigating the effects of the aforementioned consequences, the growth of installed RES introduces new problems in the grid due to the stochastic behavior of their prime mover e.g., sun and wind [6]. Indeed, it is more difficult to deliver constant power following the loads demand when the power production is not constant. For this reason and due to the increase of efficiency and reliability and the decrease in the cost of power electronics, converters have been largely deployed [7]. Moreover, using the proper control strategies is possible also to improve the power quality e.g., doing voltage harmonics compensate on [8].

For what concerns the burden on the main grid, since the improvement of the transmission network is economically challenging, a cost-effective solution has been found in Microgrids or Minigrids [9], [10]. In fact, as the name suggests, the MG works like a small-scale grid and is able to provide electricity to the loads. Moreover, it lets the power produced by the DG units flows directly to the loads without having to pass through the transmission network, avoiding more losses. In **Fig. 1.1** the general structure of a microgrid is depicted. In this structure, as can be seen, RES such as PV panels micro-turbines, and fuel cells, also, diesel generators are used to deliver the electricity to the load. Nevertheless, to provide constant power to the loads in spite of the stochastic behavior of the RES, Energy Storage Systems (ESSs) are embedded in the system [11].

The energy sources are connected to a common bus by mean of converters so that the power can flow either to the loads and to the storage systems when needed or to the grid when the produced power exceeds the needs of the MG. In fact, the microgrid is capable to operate in two modes: connected to the grid and disconnected from the grid. They are commonly referred as grid-connected

mode and islanded mode respectively. When connected to the grid, the MG acts as a load/source and its main duty is the control of the output power, since the voltage at the Point of Common Coupling (PCC) and the frequency references together with the balance between produced and demanded power are managed by the main grid. When the MG is in islanded mode, its control is more complex because it has to perform voltage and frequency control and has to take care about the balance between supply and demand, the power quality, and the communication between the several components of the MG [12], [13]. To switch between states, a Static Transfer Switch (STS) is used. It is a smart switch able to recognize, after the evaluation of grid's and MG's status based on feedback measurements, whether the MG should be connected or not to the transmission network [14].

As can be inferred from the previous analysis, the integration of DGs and ESSs with the MGs not only ensures to lighten the burden on the main grid but also allows to cope with the penetration of RES. This cooperation is particularly advantageous since it provides higher reliability and flexibility to the grid. For instance, the possibility of intentional islanding is useful when e.g., there is a fault in the grid since the MG can still operate thanks to the presence of several DGs and ESSs [11] so that the loads are always supplied. Looking further ahead, a massive diffusion of MGs would be beneficial with respect to the concept of a smarter, more efficient, reliable, and technologically advanced grid, known as Smart Grid (SG) [15].

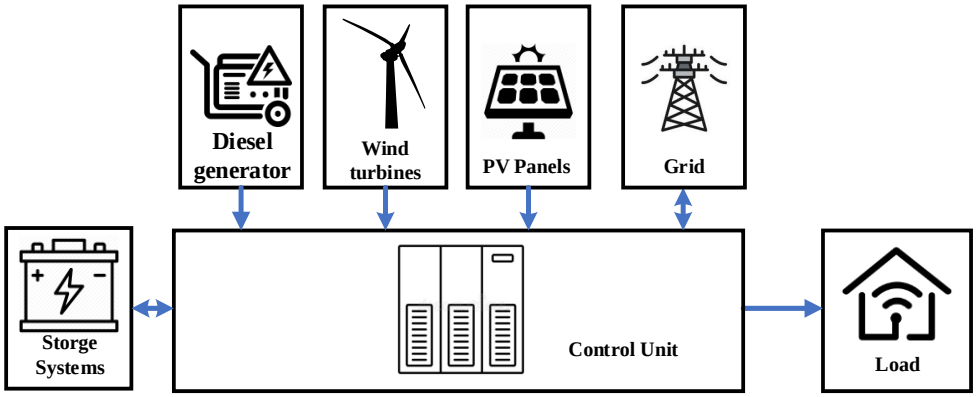


***Fig. 1.1**. Conceptual scheme of a Microgrid.*

On the other side, due to the bidirectional power flow introduced by the use of DGs, different protections are needed, since the previous ones installed were conceived for a unidirectional one: from the big power plants through the transmission and distribution lines to the loads. Moreover, while in big power plants the initial energy needed by new loads is provided using the energy stored in the generators' inertia, in the micro sources, since they are inertia-less, the introduction of new

loads leads to power unbalances between generation and loads that need to take care about [16], [17]. Finally, also regulatory issues related to the grid connection of DGs need to be faced [18].

Going further, depending on the type of the common bus it is possible to have DC, AC, or hybrid Microgrids [19], as shown in **Fig. 1.2.**

Hereafter a thorough analysis of the peculiarities and the feasibility of each type of Microgrid is carried out. The AC Microgrid offers the opportunity to integrate DGs to the grid in a straightforward way avoiding significant modifications [20]. Furthermore, due to the widespread range of protections on the market is possible to achieve a high fault management capability. Moreover, voltage levels can be easily modified using low-frequency transformers. Nonetheless, the AC architecture presents some downsides like the need for synchronization by the DGs and the reactive power circulation that causes losses in the network grid.

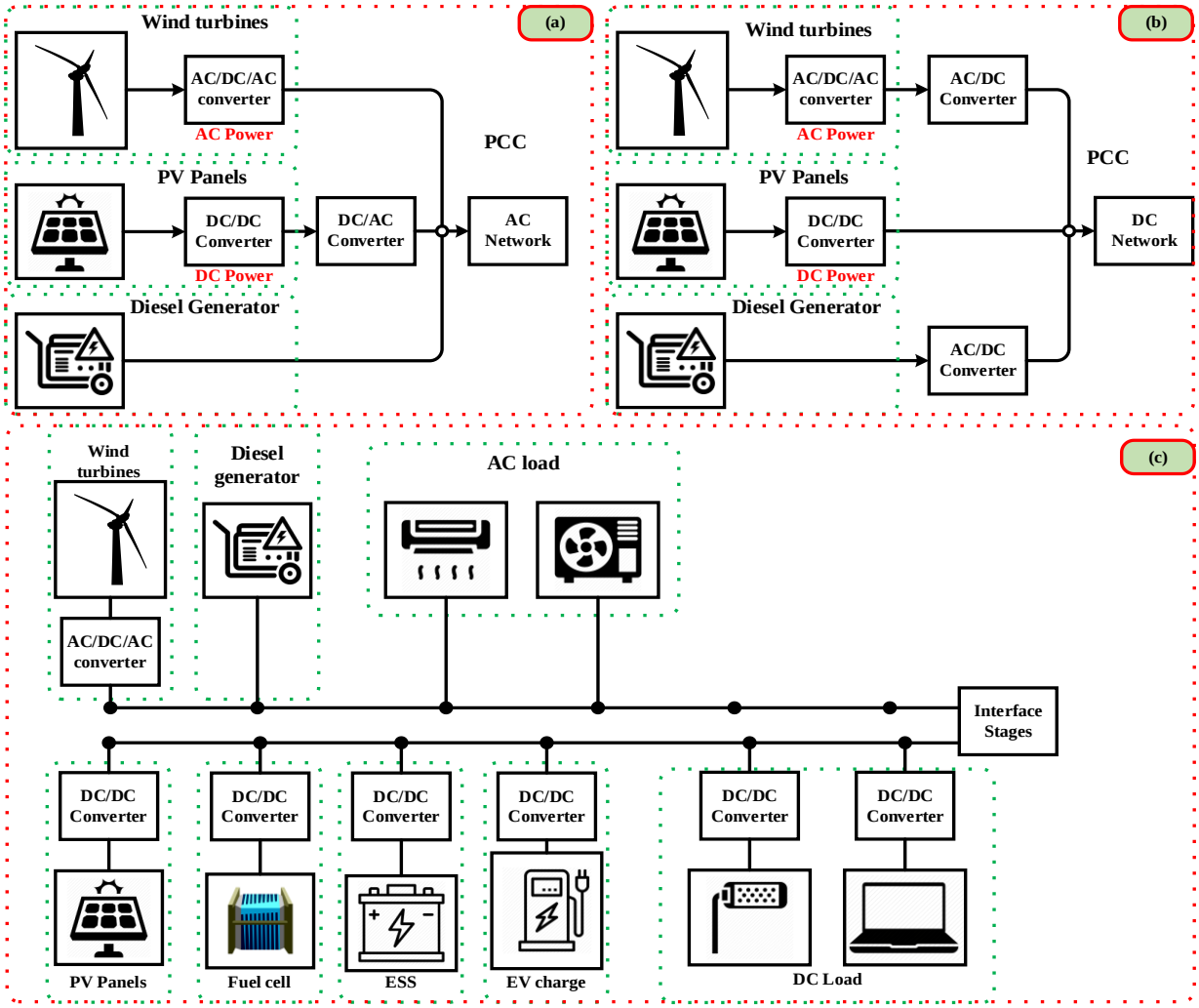


Fig. 1.2. Types of Microgrid.

Moving to the DC microgrid, it is more efficient concerning the AC one as fewer converters are needed and, because there is no reactive power production, no reactive current is circulating in the grid. Additionally, for the connection of DGs, no synchronization process is needed. Anyway, the adaption of the distribution grid to the DC system implies consistent investments. Finally, for what regards the Hybrid MG, it combines the advantages of both AC and DC MGs, having a network for each MG type ensuring the direct integration of DGs, ESSs, and loads to the AC or DC network respectively. At the same time, the protection aspect for the DC MG network is a problem, as mentioned before. Furthermore, also the management of such a structure is more complex due to the control needs of the devices connected to the AC and DC networks and also the control of the interface power converter [21].

Due to the ease of integration within the existing transmission network, in this project, the focus is on the AC MGs

1.2 Architecture of a Microgrid

The fundamental elements of a Microgrid can be possible to identify its which are the distributed generator (or prime movers), the energy storage devices, the control unit, and the loads. As an example, resuming **Fig. 1.1**, the aforementioned elements are highlighted, resulting in **Fig. 1.3**. Starting from the prime movers, they are the energy sources and their type depends on the geographical configuration and raw material availability. The first affects the RES that can be used, i.e. wind turbine, PV panels, tidal or wave power, and so on; the latter determines the type of non-renewable energy employable, like diesel generators, fuel cells, microturbines, etc. From the energy efficiency and the integration of RESs point of view, the ESSs contribute in a major way. They allow energy storage when there is an over-production and give the possibility to consume it when a power shortage occurs. Depending on the medium and on the conversion process, there are different storage technologies: chemical, electrochemical, mechanical, electrical, and thermal storage. Nowadays the most used energy storage system is the pumped hydro [22], even though due to the spreading of DERs lead-acid and Lithium-ion batteries are gaining more and more popularity [23]. Furthermore, the researches around flywheels and supercapacitors are generating interesting results [24], [25]. For a more detailed overview of the existing storage systems and their growth perspectives check [26].

Moving forward with the analysis of the basic elements in a Microgrid, there are loads. They can differ from each other depending on the power needed, i.e., a private house, a commercial building, or a factory. Another way to distinguish the loads is the need for continuity of electricity. Just think

about the differences between the needs of a private house or a hospital or a data center. In the last two cases the power supply must be guaranteed in order to ensure in the hospital case the possibility to assist the patient and be able to carry on a surgery; while in the data center case, a blackout can cause the loss of sensitive data. One more criterion to classify the loads is by their linearity. Indeed, if a load changes its impedance with the applied voltage, it is defined as non-linear. This implies that the current drawn by the load contains harmonics that make it non-sinusoidal even when the non-linear load is connected to a sinusoidal voltage. Furthermore, the harmonic currents, interacting with the grid impedance, will cause voltage distortions [27].

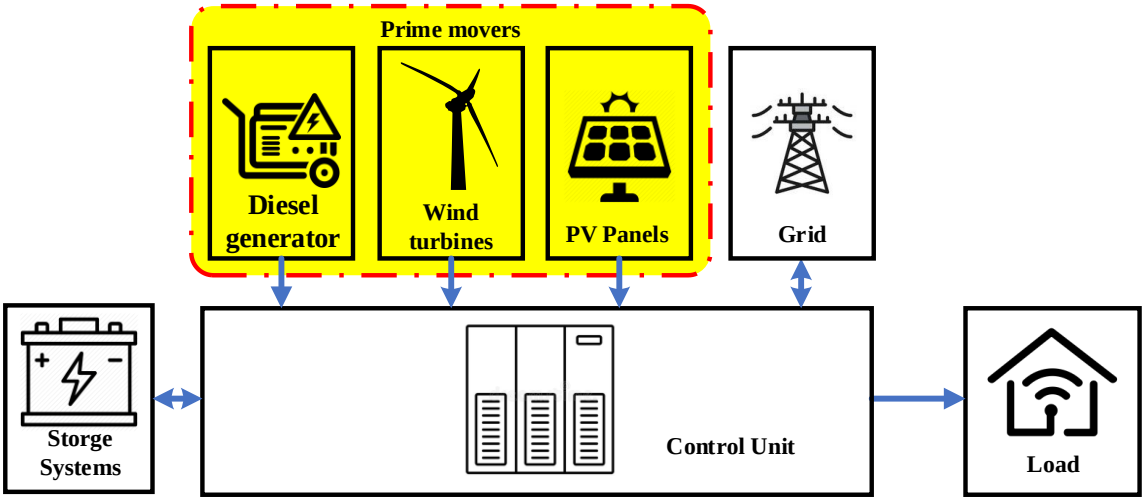


Fig. 1.3. *Fundamental components of an AC MG.*

The interactions between all the system components have to be coordinated so that the MG can satisfy the constraints about power quality, power exchange with the grid, safety, etc. This is the duty of the control unit that, from a hardware point of view, can be either a Digital Signal Processor (DSP) or a Field Programmable Gate Array (FPGA). The choice of the hardware of the control unit depends on the size, the control complexity, and the processing power needed by the MicroGrid. An element that is significant and plays a key role but is not highlighted in **Fig. 1.1** is the protection system. Indeed, the presence of distributed energy sources in nowadays medium- and low-voltage network made necessary an upgrade of the protections used until now. This because in the past, the distribution system was conceived as a radial network, delivering power from the substations to the customers, resulting in unidirectional power flow. In this system, the coordination of the circuit breakers through the use of overcurrent relays, reclosers, and fuses was clearly defined. Nowadays instead, the deployment of DGs implies that the distribution network is no longer radial but has become active. For these reasons, different approaches from the protection point of view have been developed and

are still a hot research topic as can be seen in [28]. Once the basic elements that characterize a Microgrid have been analyzed, it is interesting to see how the Microgrid interacts with the main grid in the two possible cases, namely the Islanded and the Grid-Connected mode [29].

1.3 Microgrid Operation Modes

As mentioned in Section, one of the peculiarities of the Microgrid is that it can operate either while connected to the grid or as an energy island. This thanks to the possibility of using the VSI in the so-called Voltage Controlled Mode (VCM) and Current Controlled Mode (CCM). When operating in VCM, the output voltage of the VSI is controlled, modulating its amplitude and frequency. In the CCM instead, the output current is regulated to the reference value. Furthermore, the transition from one operational mode to the other can be done seamlessly. In this section, the features of both operating modes are described.

1.3.1 Islanded Mode

When the Microgrid is not connected to the main grid, it is said to be in an islanded mode. There are different scenarios where the islanded operation can be particularly advantageous. One of them is the electrification of places geographically difficult to reach or where the distance from the main grid is so big that the costs of the grid connection are too high compared to the incomes for the Distribution System Operator (DNO). In this case, the islanded operation is the best option in order to give access to electricity to the customers [30]. Another interesting scenario when the islanded-mode is not only advantageous but even crucial is when a grid fault occurs. In this case, through the continuous monitoring of the grid status, the STS detects the extraordinary condition and disconnects the MG from the main grid, assuring the continuity of supply to the local loads and protecting distributed generators and storage systems. Doing so, the grid reliability is improved as well as its capability to reduce the number of consumers that experience the voltage outage. It is worth to notice that the STS opens and lets the MG starts the islanded operation not only when a fault occurs, but also when the grid is weak, guaranteeing the power quality needed by the loads to work properly [31]. Following up on the correct operations of loads and generators, when in islanded mode, the Microgrid has to carry out duties that normally are pursued by the main grid:

- Voltage and frequency control so that both are within the limits. The typical accepted deviation for the voltage from its nominal value is ± 5% while for the frequency is ±2%;

- Power balance. This means that the amount of power produced by the DERs has to match with the amount of power needed by the loads. If there is a mismatch and there is an overproduction, ESSs can be a good solution. Nevertheless, if there is an underproduction, the voltage will drop, causing power outages and eventually a blackout;
- Power quality. This aspect is fundamental when it comes to supply the loads. In fact, if the voltage supplied is not within the voltage and frequency limits above mentioned and its Total Harmonic Distortion (THD) is higher of a threshold value, typically 5%, then the loads can malfunction, fail prematurely or not operate at all.

In order to be able to ensure the above-mentioned properties, there is the need to use some interface inverters for the distributed generators in the Microgrid in voltage-controlled mode: the output voltage of each converter is modulated in amplitude and frequency (staying within the imposed thresholds), in order to provide the requested power.

In this way, even though some DERs' work in Current Controlled Mode (CCM), i.e. PVs and small wind turbines, to extract the maximum power from their energy source, the respect of the voltage amplitude and frequency thresholds is assured by the VSIs working in VCM.

1.3.2 Grid-Connected Mode

When the Microgrid is in grid-connected mode, it can either import power from the main grid or supply power to the distribution network, acting as a controllable load or as a controllable source. Further, the main utility grid imposes the active and the reactive power flow of the Microgrid so that the power imported from the grid is minimized [32]. Then, these commands are managed by the MG's control unit and, by mean of communication buses, given to the DERs according to their power ratings. The goal is to produce most of the power in loco to reduce the burden on the distribution grid and consequently the losses in the energy transmission.

1.4 Microgrid control

This section discusses the MG control approaches that can specified in two main approaches; centralized and decentralized, as well as the MG control hierarchy, adopted in the literature, including the primary, secondary and tertiary control layers.

1.4.1 Centralized and decentralized control approaches

For Microgrids, there are two main categories of controlling them: centralized and decentralized. In the centralized approach, all the information are sent to a central controller by means of high-speed communication [33]. Furthermore, the central controller performs all the calculations and consequently commands the control actions for each DG. On the contrary, in the decentralized control, each unit has its own controller that performs calculations and gives control commands based on local measurements to the unit is in charge of, without being aware of the control actions taken by the other units [33].

1.4.1.1 Centralized Approaches

The employment of a centralized approach in the control of a Microgrid can be beneficial under several aspects. Indeed, a centrally controlled MG is easier to operate for the MG owner as all the actions that need to be taken are pursued by a central controller. In fact, after the data collection from all the components in the MG such as DERs, ESSs and eventual controllable loads and an analysis of the energy prices in the market, the central controller performs all the calculations to optimize the energy production and consumption inside the MG and the power exchange with the main grid [34]. Further, the Microgrid central controller has also to act in order to meet the power quality requirements given by the grid codes.

The above-mentioned characteristics make the centralized approach particularly suitable when:

- The owners of the DERs and the loads are pursuing common goals and want to reach them through cooperation;
- The MG's components are concentrated, i.e. in industrial or commercial Microgrids.

However, when the DERs are dispersed, there is a need for high bandwidth communication in order to guarantee a good system dynamic response. This can be difficult to realize or, if possible, has a high cost. Furthermore, also the system reliability is decreased by the use of a centralized control since if the central controller experiences a fault, the whole MG won't be able to work.
Among the most known centralized control methods there are:

- Master & slave: on one inverter, in VCM, there is the central controller (master) that performs all the calculations and gives the power, voltage and frequency commands to the other inverters (slaves), in CCM. If the master fails, a slave unit will become the master, in order to avoid the system overall failure;

- Average Load Sharing: the average current is sensed by means of a single wire with a properly chosen resistor connected to the current sensor for each converter.

In this case, low-bandwidth communication can be used, but the current harmonics can circulate;

- Circular chain control (3C): the current reference of each module is taken from the module before, after sensing the inductor current, forming a control ring.

1.4.1.2 Decentralized Approaches

Unlike the centralized approaches, when the Microgrid is controlled in a fully decentralized way, each DG and ESS has its own controller that works independently, based just on local measurements [35]. As a consequence, the distributed energy sources have the plug-and-play capability, since they do not create any disturbance to the other DGs, increasing the reliability of the system. Nonetheless, a fully decentralized approach is not feasible for the control of several DGs due to the strong coupling between the operations of the units in the system. Therefore, a minimum level of communication in order to coordinate the operations of the inverters is needed [36].

1.4.2 Microgrid hierarchical control

A good compromise between the fully decentralized and the fully centralized approaches is the hierarchical control. It is structured in three levels, namely primary, secondary, and tertiary [12], [37-40]. They differ from each other based on the speed of the response and their duties. The employment of the hierarchical control makes the integration of dispersed DERs possible by means of low bandwidth communication, increasing also the system reliability and redundancy [36]. Furthermore, the plug-and-play characteristic ensured by the decentralized approach can be achieved since there are higher control levels that take of the coupling between the operations of the units in the system. In **Fig. 1.4** the general structure of the hierarchical control is presented, together with a brief overview of the main duties of each control level.

a) Primary Control

The primary control, or also known as local control, is the lowest level in the hierarchy. Its response relies solely on local measurements, without any need of communication. As basic level control, it has the fastest response to share the load among the paralleled dispatchable units based on their rated power. Furthermore, it has to have islanding detection capability and is also responsible for the improvement of voltage stability and for the reduction of circulating currents that may occur when the converters are connected in parallel [39], [41].

Among the control strategies for the primary level, the most known is the droop control, where the voltage amplitude and frequency are regulated based on the requested power, simulating the inertia of the synchronous generators in the transmission system [27], [42], [43].

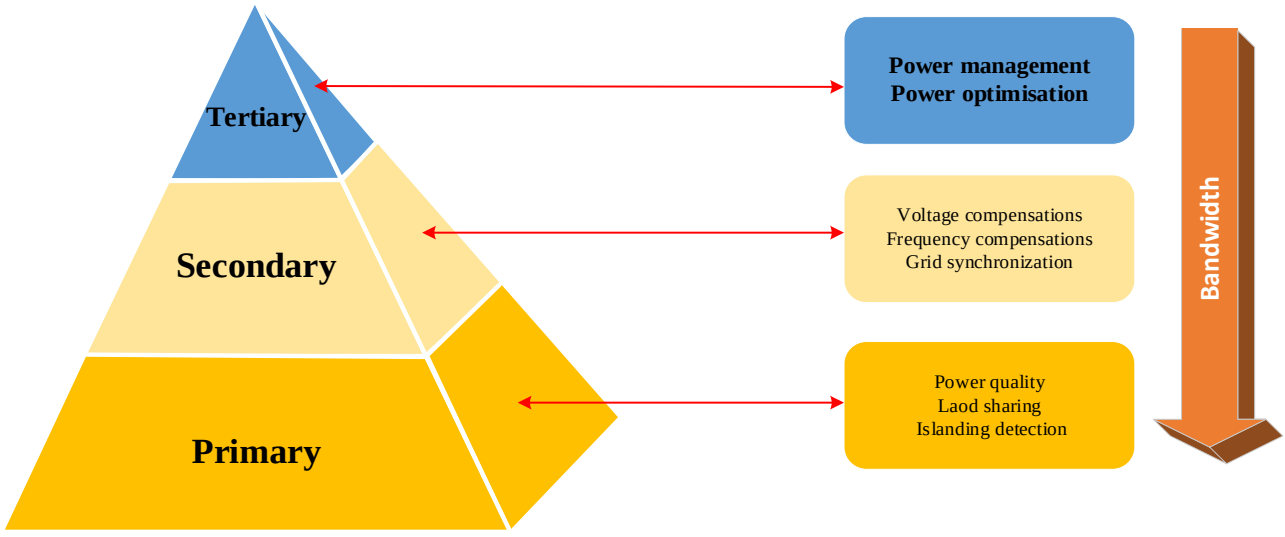


***Fig. 1.4**. Hierarchy of the control for AC microgrid including three control levels.*

b) Secondary Control

The secondary control has lower bandwidth with respect to the primary control, in order to decouple the two dynamics, but also to reduce the communication speed and to have enough time to perform all the calculations. Indeed, it compensates for the voltage and frequency deviations caused by the primary control and performs the grid synchronization [44], [45]. Moreover, the secondary control can also act as the Energy Management System, taking care of power flow and power quality within the MG, as it is the highest control level when the MG is in islanded mode [46].

c) Tertiary Control

The last, and also the slowest level of control is the tertiary control. Indeed, its control actions take place in the range of minutes. This level performs the power regulation when the Microgrid is connected to the grid [47]. Furthermore, the power references given to the secondary control can be calculated based on an optimal analysis focused on the market prices, the weather forecasting (when sources with stochastic behavior are employed, e.g., PVs) and on the agreement between the customer and the grid operator [12], [48], [49].

Actually, the focus of the present research is given to the primary control based the droop control for single-phase parallel-connected VSIs in islanded AC MG. Hence, an overview of the primary control level, considering the included control loops within is presented in the following section.

1.5 Droop control based-primary control of MG

This section presents the state of the art regarding the primary control and the included control loops within, i.e., droop control and power calculation loops, virtual impedance control loop, and the inner control loop.

The primary control, is a local decentralized controller, which is responsible for the reliability and improving the MG system performance and stability; meanwhile adjusting the frequency and the amplitude of the inverter output voltage to get the reference of the inner multiloop controller, and for ensuring an accurate active and reactive power sharing between parallel-connected DG units. Each inverter has its own control loop usually has an external power control loop based on the droop method that allows each DG unit to operate autonomously and any communication links among the DG units in a MG are required [50]. The schematic diagram of the primary control structure is shown in **Fig. 1.5**, which comprises two main blocks; the power-sharing controller, and the inner controller. The power-sharing control includes the power calculation block, the droop controller, and the virtual impedance control loop. The power calculator is in charge of computing the averaged value of the active and reactive powers. The droop control method is introduced to generate the frequency and amplitude references according to the computed active and reactive powers. The virtual impedance control loop is used to extract the virtual impedance voltage to be added to the voltage reference, generated by a sinusoidal reference generator using the droop references, to produce the output voltage reference of the inverter. The inner controller regulates the inverter output voltage to the provided reference.

Since the microgrid can operate in islanded or grid-connected modes, it makes the power sharing strategy varies drastically. These characteristics make primary control-based on the droop method a popular research topic. Many survey papers have been published in this area [42], [51]- [54], in which the main contributions on primary control are focused on improving transient response, stability, active and reactive power sharing, harmonic power sharing, virtual impedance control, estimation performance and others. However, the performance enhancement of this control level can be achieved by improving the performance of one of the included control units within. In this regard, the working

principle, mathematical formulation, and the reported research in the literature survey of each control unit regarding performance enhancement are presented in the following paragraphs.

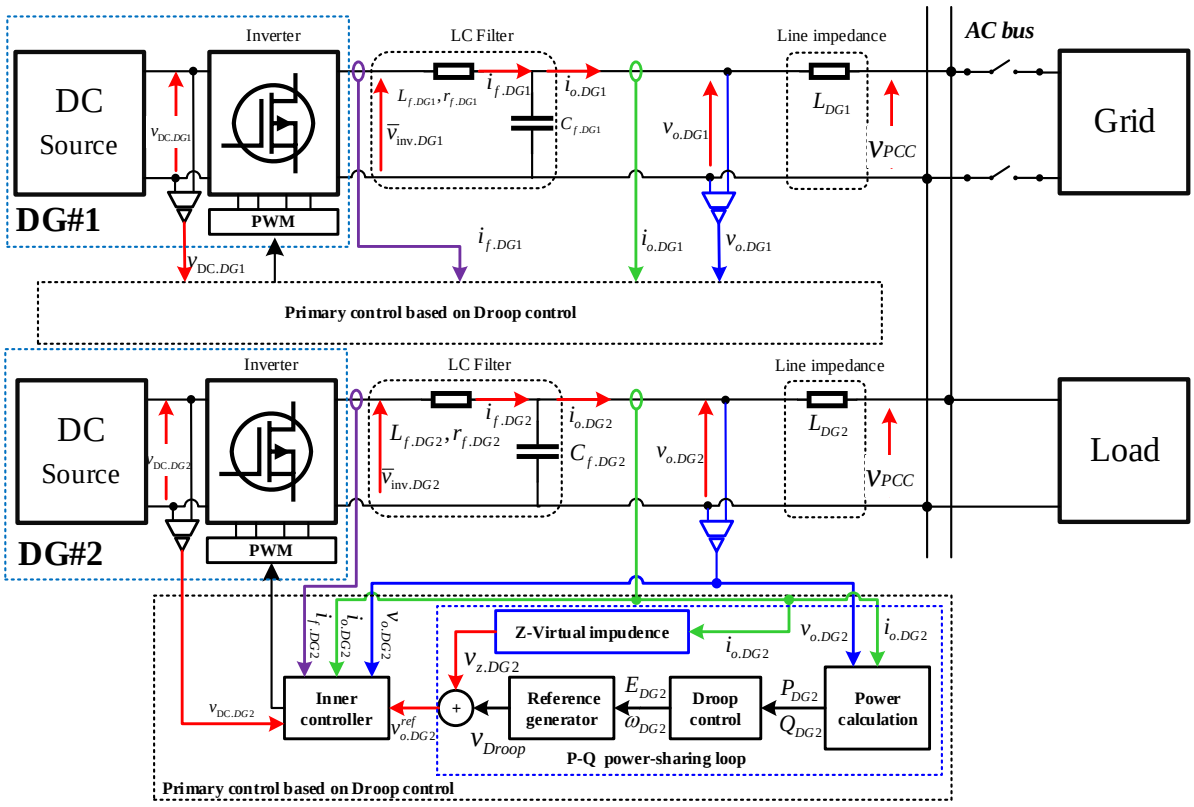


Fig. 1.5. *The primary control scheme for two single-phase DGs connected in parallel to an AC bus via a line impedance. Each DG consists of a DC source associated with a VSI with an LC filter and has an independent local controller. The load and the main grid are, also, linked to the AC bus.*

1.5.1 Droop control loop

The droop control strategy has been widely adopted to coordinate the DG units within a microgrid due to the no need for critical communication among parallel-connected DG units [55]. The main objective of the droop control is ensuring the power sharing between the grid-forming converters operating in the microgrid. The idea of the voltage and frequency droop control, in an inverter dominated-microgrid, comes from the conventional synchronous generators in large interconnected power systems. A droop characteristic control performs the coordination of generators with a frequency/active power and voltage/reactive power droop characteristics, in order to share the active and reactive power demand in a MG. The same concept is adopted in this technique to control the active and reactive power flow by adjusting the frequency and amplitude of the output voltage. In

fact, the frequency-active power (***f-P***) and voltage-reactive power (***E-Q***) relationships can be reached through the following mathematical analysis.

Fig. 1.6 shows the equivalent circuit of two single-phase inverters connected to an AC bus through decoupling impedance, in which every inverter stage is modelled as a sinusoidal voltage source with an output impedance in series.

According to **Fig. 1.6**, the expression of the output current ($\boldsymbol{I_i}$) of an inverter can be derived as follows:

$$I_i = \frac{E_i \angle \varphi_i - V_{PCC} \angle 0}{Z_i \angle \phi_i} = \frac{E_i}{Z_i} \angle (\varphi_i - \phi_i) - \frac{V_{PCC}}{Z_i} \angle -\phi_i \tag{1.1}$$

where $\boldsymbol{E_i \angle \varphi_i}$ is the inverter open-circuit voltage, $\boldsymbol{V_{PCC} \angle 0}$ is the common bus voltage, and $\boldsymbol{Z_i \angle \phi_i = R_i + jX_i}$ is the inverter to the common bus impedance, which considers the inverter output impedance and the line impedance of the connection wires.

Besides, the complex power $\boldsymbol{S_i}$ drawn to the AC common bus from each inverter can be expressed as follows:

$$S_i = (V_{PCC} \angle 0)\,\bar{I}_i = P_i + jQ_i \tag{1.2}$$

Therefore, the averaged active $\boldsymbol{P_i}$ and reactive $\boldsymbol{Q_i}$ power of each inverter can be deduced as follows:

$$P_i = \frac{V_{PCC}}{Z_i}\left(\left(E_i \cos(\varphi_i) - V_{PCC}\right)\cos(\phi_i) + E_i \sin(\varphi_i)\sin(\phi_i)\right) \tag{1.3}$$

$$Q_i = \frac{V_{PCC}}{Z_i}\left(\left(E_i \cos(\varphi_i) - V_{PCC}\right)\sin(\phi_i) - E_i \sin(\varphi_i)\cos(\phi_i)\right) \tag{1.4}$$

These expressions can be simplified if we consider that the phase difference $\boldsymbol{\varphi_i}$ (i =1, 2) between the inverters output voltages and the common bus, are very small, which is true because the inverters are first accurately synchronized to the common bus voltage before the connection to the common bus.

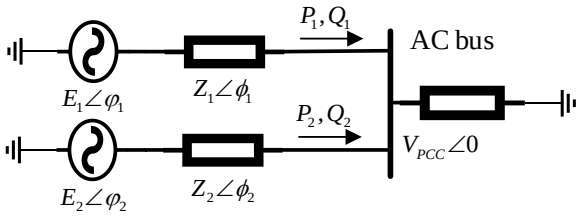


Fig. 1.6. *Equivalent circuit of two DG units connected to common AC bus.*

Considering the above assumption, $\boldsymbol{\varphi_i}$ is very small, i.e., $\boldsymbol{\sin \varphi_i = \varphi_i}$ and $\boldsymbol{\cos \varphi_i = 0}$, Eqs. (1.3) and (1.4) can be simplified to:

$$P_i = \frac{V_{PCC}}{Z_i}\left(\left(E_i - V_{PCC}\right)\cos\left(\phi_i\right) + E_i\varphi_i \sin\left(\phi_i\right)\right) \quad (1.5)$$

$$Q_i = \frac{V_{PCC}}{Z_i}\left(\left(E_i - V_{PCC}\right)\sin\left(\phi_i\right) - E_i\varphi_i \cos\left(\phi_i\right)\right) \quad (1.6)$$

With these last expressions, it can be noticed that $\boldsymbol{P_i}$ and $\boldsymbol{Q_i}$ depend simultaneously on the system impedance phase angle $\boldsymbol{\phi_i}$ and the difference between the inverter output voltage and the common bus voltage $(\boldsymbol{E_i - V_{PCC}})$ [55]. In this regard, the active and reactive powers can then be particularized to three kinds of possible system impedances; mainly inductive, mainly resistive, and complex impedance. For DG systems, in which the impedance is usually purely inductive, i. e., $\boldsymbol{X_i \gg R_i}$ and $\boldsymbol{Z_i \angle \phi_i \cong X_i \angle \pi/2}$, hence, Eqs. (1.5) and (1.6) become:

$$P_i = \frac{E_i V_{PCC}}{X_i}\varphi_i \quad (1.7)$$

$$Q_i = \frac{\left(E_i - V_{PCC}\right)V_{PCC}}{X_i} \quad (1.8)$$

where $\boldsymbol{X_i}$ is the output reactance of an inverter.

Based on the relationships of Eqs. (1.7) and (1.8), we note that the inverter active power $\boldsymbol{P_i}$ relies directly on the phase angle $\boldsymbol{\varphi_i}$, while the reactive power $\boldsymbol{Q_i}$ depends on the amplitude voltage $\boldsymbol{E_i}$. Therefore, the phase angle $\boldsymbol{\varphi_i}$ and the amplitude voltage $(\boldsymbol{E_i - V_{PCC}})$ can be used to control the amount of active and reactive power demand in the MG, respectively. As a result, the droop control strategy used in parallel inverters system introduces proportional droops in the amplitude $\boldsymbol{E_i}$ and frequency $\boldsymbol{\omega_i}$ of the inverter output voltage as following:

$$\omega_i = \omega^* - nP_i \quad (1.9)$$

$$E_i = E^* - mQ_i \quad (1.10)$$

where $\boldsymbol{\omega^*}$ and $\boldsymbol{E^*}$ correspond to the nominal frequency and amplitude output voltage at no load, and $\boldsymbol{n}$ and $\boldsymbol{m}$ the frequency and amplitude droop coefficients, respectively.

Eqs. (1.9) and (1.10) defines the functions of the droop controller which can balance the active and reactive powers by instantaneously changing the inverter frequency and amplitude. Accordingly,

to these expressions the droop control can be implemented as shown in the schematic diagram of **Fig. 1.7**. From this figure, the droop method is implemented by three control blocks; the power calculation, the droop equations, and the sinusoidal generator. The outputs of the droop block are processed by the sinusoidal generator to produce the inverter output voltage reference, which can be defined as:

$$v_{Droop.i}(t) = E_i \sin(\omega_i \times t) \tag{1.11}$$

The droop control characteristics are presented in **Fig. 1.8**. It can be seen that, when the active power flow increases due to the increase in load demand, the frequency of an inverter drops. Similarly, the voltage amplitude drops when the reactive power increases. The droop gains, ***m***, and ***n*** are represented by the slope of the line in **Fig. 1.8**. These gains (***m*** and ***n***) can be determined by the maximum frequency and voltage deviations ($\Delta\boldsymbol{\omega_{max}}$ and $\Delta\boldsymbol{E_{max}}$) and the inverter active and reactive power rating $\boldsymbol{P_{rated}}$ and $\boldsymbol{Q_{rated}}$, i.e.,

$$n = \frac{\Delta\omega_{\max}}{P_{rated}}, \quad m = \frac{\Delta E_{\max}}{Q_{rated}} \tag{1.12}$$

It is worth noting that the allowed maximum frequency and voltage deviations according to the IEEE standards are at 2% and 5%, respectively [98].

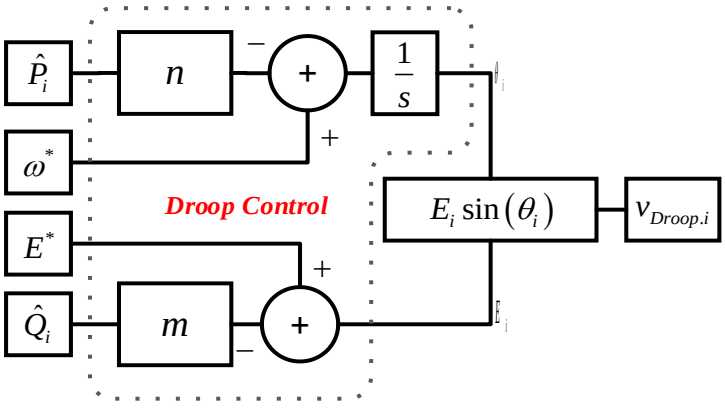


Fig. 1.7. *Block diagram of the droop control loop.*

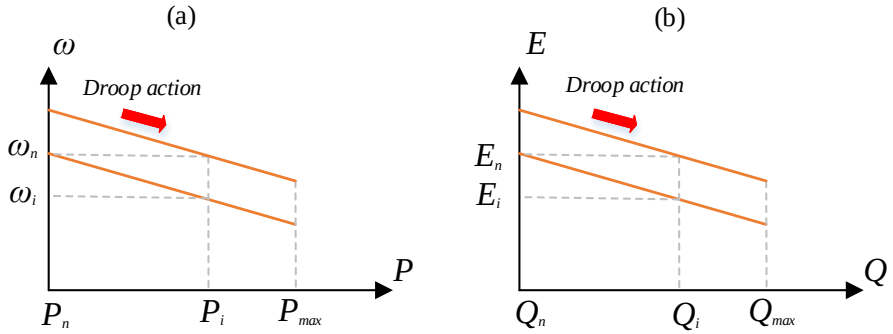


*Fig. 1.8. Droop characteristics; (**a**) frequency–active power, (**b**) voltage–reactive power.*

The conventional droop method; of **Fig. 1.7**; has been widely used in single-phase islanded microgrids [51], [52], [56]. However, these conventional methods suffer from several drawbacks, such as, poor reactive power sharing, and stepper droop ensures good power sharing but result in degrading the voltage frequency and voltage regulation performance; this is the inherent tradeoff of the droop control [12]; and may cause instability issues in the microgrid. To overcome these issues and ensuring accurate power sharing, researchers have developed several improved droop control methods applied to islanded AC MGs [52, 53], [57-58]. In [57], an adaptive voltage droop scheme with modified laws is suggested, in which two terms are incorporated to the conventional reactive power control. The first term, in this method, is employed to compensate for the voltage drop across the transmission lines, while the other term is introduced to hold the system stability and enhance reactive power sharing. The transient response of the microgrid is improved by determining the gains of the added terms in an adaptive manner. Paper [58] proposes a new droop control scheme consider ***P-Q-V*** relationship for MG systems with complex impedance. This method facilitates simultaneous active and reactive powers control, in which the droop coefficients are adjusted online through a lookup table. The proposed ***P-Q-V*** droop control has offer accurate power sharing with good dynamic performance, More works in this area can be found in [59], [60], and [61].

On the other hand, to carry out the droop functions expressed at **Eqs. (1.9)** and **(1.10)**, it is necessary to compute the averaged active and reactive powers of inverters over one line cycle. This is usually done by the means of LPFs with a very low cut-off frequency after calculating the instantaneous powers [62]. This effect forces the droop method to operate at a very low dynamic velocity and degrades the system stability. Therefore, different solutions for power calculation have been proposed in the literature to improve the droop control dynamic velocity and performance at steady state [63-67]. Among these solutions, schemes based on the SOGI-FLL technique, which used to estimate the fundamental orthogonal components of the inverter current and voltage, which in turn

employed to compute the averaged active and reactive in ***αβ*** frame [66], [67]. In addition, other methods use the SOGI technique as a filter to cancel the double frequency result from the product of the voltage and current [68]. These methods have ensured ***P/Q*** calculation with fast dynamic response speed and good accuracy at steady state but in their study, they only consider the case of linear load sharing. In the case of nonlinear loads, where a highly distorted current is expected, these methods cannot provide effective ***P/Q*** calculation, hence, the MG may subject to instability issues. To solve with this problem, advanced power calculation approaches for improving the performance of the droop method have been suggested. In [69], a method based on the discrete Fourier transform (DFT) has been proposed for computing ***P*** and ***Q***. In addition, a Least Mean Squares (LMS) approach for obtaining the averaged powers has been developed in [70]. Papers [71] and [72] have discussed approaches incorporating schemes-based, DSOGI, MSOGI and n-SOGI [73]. The main objective of these approaches is achieved a faster and accurate calculation of the averaged powers to improve the droop control performance, hence, the system stability.

It is worth noting that the estimation block is, also, essential in MG systems, in order to determine the key parameters such as, frequency, phase, and amplitude and output voltage components. The PLL is widely used in MG as estimator of the key parameters. However, in order to improve the performance of the microgrid control system an accurate estimation of these parameters is required. In this regard, various schemes with improved features have been proposed in the literature, among them EPLL, ESOGI-FLL, and etc., to achieve system performance enhancement. More details about the estimation unit will be given in Chapter 2.

1.5.2 Virtual output impedance loop

As the transient and steady-state behaviors of the droop method are highly dependent on the system mismatches, that can affect the inverter output impedance accuracy, and the line impedance of the wires used to perform the connection of the inverter [54], [74]-[75]. The virtual impedance control loop is introduced to decouple the active and reactive power flow and to improve the overall output impedance of each DG unit. Besides, the introduction of the virtual impedance into the droop method-based control can avoid the circulating harmonic current between VSIs, therefore, improve the accuracy of the reactive and harmonic power sharing, especially in the case of supplying nonlinear loads. In fact, the virtual impedance loops is implemented by including fast control loops in the droop control method, as shown in **Fig. 1.9.** Accordingly, the expected voltage can be modified [74], as:

$$v_o^{ref}(s) = v_{droop}(s) + z_v \times i_o(s) \quad (1.13)$$

where z_v is the virtual output impedance, and v_o^{ref} is the output voltage of the inverter.

The equivalent circuit of a DG unit with virtual impedance is shown in **Fig. 1.9**, in which the virtual impedance is usually wired in series with the resistive line impedance to make the overall output impedance of the DG inductive, this in turn improves the stability and transient performance of the system.

In AC MGs, the line impedance and the output impedance of the inverters are usually considered to be mainly inductive, this can be achieved by drooping the output voltage proportionally to the derivative of the output current with respect to the time, i.e., $z_v(s) = sL_v$ (L_v is the virtual inductance). However, this is not always true since the inverter output impedance also depends on the adopted inverter control strategy and the system parameters [74]. In addition, the adopted conventional methods for the implementation of virtual impedance, such as in [76], can be highly affected by the output-current inherent noise and distorted by any kind of nonlinear loads. Therefore, improved virtual impedance implementation considering inductive, resistive, and complex impedances to fix the output impedance of the inverter have been proposed [77]. One of the recent of them, the implementation of the virtual impedance at the fundamental and selected harmonic frequencies that developed in [78] and [79]. Another method presented in [80], which proposes virtual impedance implementation based on the MSOGI algorithm for introducing the harmonic virtual impedance. These methods can alleviate voltage distortion problems caused by harmonic loads and as a result improve the power sharing features.

It is worth noting that proper design of the virtual resistance and inductance is important for appropriate mitigation of the coupling between ***P*** and ***Q***.

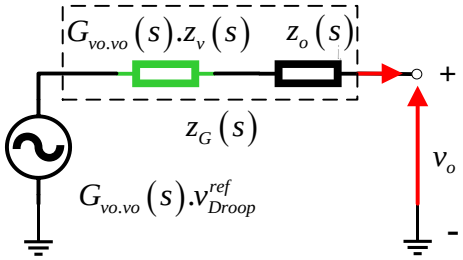


Fig. 1.9. *Equivalent circuit of a VSI with virtual output impedance.*

1.5.3 Inner voltage and current control loops

The inner control loop is designed to regulate the inverter output voltage to the desired voltage reference; provided by the droop control, while maintaining the system stable. This control scheme is consisting of voltage and current control loops, as presented in **Fig. 1.10**. Classical PI regulator is most commonly employed technique in these loops to control the capacitor voltage and inductor current in each DG unit and to reach fast transient response [12], [50]. However, the design of the inner control loops is very important for the MG performance. Different techniques have been applied for the control of VSI in islanded microgrid. For example, in [81] a Proportional resonant (PR) controller adjusted at the fundamental frequency for paralleled single-phase droop-controlled inverters was proposed in order to improve the output voltage-tracking feature. In addition, a scheme of the inner loop voltage controller based on MCS-MPC technique has been developed in [82], in order to improve reference tracking, and eliminate the steady state error. Further, paper has developed. Further, sliding mode technique has been established for the inner loop in [83], for improving the reference tracking speed as well as a non-overshoot transient performance in islanded MG.

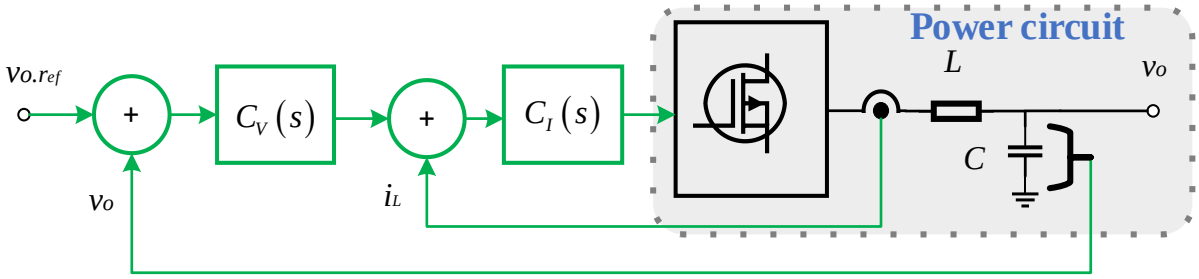


Fig. 1.10. *Diagram of double-loop control of the output voltage.*

On the other hand, the modeling and tuning procedures of the inner control loops are important for analyzing the system stability and performance enhancement. Various works related to the modeling and design of the inner control have been proposed in the literature review such as presented in [74] and [84-85].

Generally speaking, one can be concluded from the reported review, that all the developed approaches focus on providing solution to curb the major drawbacks of droop-based control i. e., instability issues due to sudden load perturbation, poor transient response, inaccurate load sharing and improving power sharing performance even under highly harmonic distortions due to nonlinear operating condition. To this regard, the development and design of improved primary control scheme,

regarding the estimation unit, power calculation block, virtual impedance control loops, which can ensure accurate power sharing, large stability margin and fast transient response, as well as intrinsic control of harmonic components suitable for highly distorted nonlinear load, is essential. This concept is the focus of the present thesis.

1.6 Thesis Objectives

1.6.1 Global Objective

The main objective of the present thesis is the development of advanced schemes of the included control loops within the primary control, in order to improve the power sharing among paralleled droop-controlled VSIs in single-phase islanded MG, even in the case of supplying nonlinear load.

1.6.2 Specific Objectives

In particular, the research objectives set are:

- To design an enhanced SOGI-FLL suitable for DC-Offset rejection in order to offer accurate estimation of the key parameters of a single-phase VSI-based microgrid;
- To provide mathematical analysis that allow to assess the ability of the proposed ESOGI-FLL in estimating/rejecting the DC component from a single voltage signal;
- To investigate the performance of the proposed enhanced scheme to offer effective and efficient parameter estimation under different operating conditions;
- To design, model and analyze the inner current and voltage loops and provide a guideline for the tune of the controller parameters;
- To assess the performance of the designed controllers in front of voltage and current distortions;
- To propose a power sharing controls structure with enhanced performance by introducing improved schemes in it;
- To study the stability of the microgrid system incorporating the proposed control schemes based on the MESOGI-FLL strategy;
- To derive the dynamic model of the MESOGI structure regarding the expected estimates, that is not exist in the literature.
- To improve the features of the power sharing control in front of nonlinear loads operation with highly distorted current, considering DC component and sub-harmonics.

- To simulate and demonstrate the performance of the proposed control power sharing scheme in single-phase VSIs- interfaced islanded AC MG.
- To validate the control proposal in real-time operation using an experimental setup, under nonlinear load conditions.

1.7 Thesis contribution

The main contributions of this thesis can be listed as follows:

- An enhanced structure based on the SOGI-FLL technique is proposed, in order to ensure an accurate estimation of the key parameters i.e., orthogonal components, frequency, phase of the single-phase MG. The proposed scheme can estimate the required parameters with good performance under different disturbances such as DC-offset, phase jump, frequency change, voltage sags and swell. Also, this proposed scheme offers low computational burdens. Comparative simulation study is preformed showing the performance enhancement regarding key parameters estimation of the proposed scheme. Simulation and experimental test cases are carried out and the obtained results demonstrates the effectiveness of the proposed method.
- The modeling, analysis and design of the inner current and voltage control loops are developed. the models of the current and voltage closed-loops are derived. Guideline for the proper design of the current and voltage controller parameters is suggested. Simulation and experimental test and results are conducted, which highlight the performance of the inner controller.
- The thesis presents an improved power sharing control scheme for the single-phase VSIs in islanded MG to face the problem of nonlinear loads. This control scheme introduces a method to calculate the averaged active and reactive power and the implementation the virtual output impedance algorithm based on a developed scheme with enhanced performance, named Multi-Enhanced second-order generalized integrators Frequency locked-loop (ESOGI-MFLL).The M-ESOGI approach is applied to ensure accurate estimation of the fundamental components of the inverter output current and voltage as well as the current harmonics components required to calculate the active and reactive powers and the virtual impedance voltage, even in case of sharing nonlinear loads. This effect leads to a faster dynamic velocity of the droop-based load sharing capability and improving the stability. The modeling of the MESOGI scheme, which cannot be found in the literature, is derived. The analysis of the

developed schemes is presented. Simulations and experimental results are provided validating the proposed power sharing effectiveness in front of nonlinear load disturbances.

1.8 Thesis organization

The present thesis comprises five chapters. The contents of each chapter are briefly described as follows:

Chapter I introduces the microgrid concept and components. In addition, it presents the different operating modes of a microgrid, and the microgrid hierarchical, which consists of primary, secondary, and tertiary control levels. Further, this first chapter describes, in detail, the structure of the droop method based-primary control layer and the incorporated control units within, in which the main focus is given to the droop method. The droop control and the other included control loops concepts and the mathematical developments are presented. Moreover, this chapter reports the literature review of these control units. The thesis objectives, contribution, and the outlines are introduced, also, in this chapter.

Chapter II proposes an enhanced scheme based on the SOGI-FLL technique; with DC component rejection/estimation capability; to estimate the key parameters of a single-phase microgrid system considering the worst case of a highly distorted voltage. An overview of the basic structure of SOGI-FLL as well as the mathematical development analyzes the effect of the DC-offset in the SOGI-FLL estimates are stated. The proposed Enhanced SOGI-FLL scheme (ESOGI-FLL), and the mathematical analysis highlighting the elimination of the DC-offset effect from the expected outputs are developed, also, the stability analysis of the proposed scheme is demonstrated. A comparative study regarding the computation burden of the proposed scheme with the standard SOGI-FLL and TOGI methods is presented. Simulation and experimental tests are explained and the obtained results are discussed in this chapter.

Chapter III presents the demonstration of the inner control loop, represented by a dual-loop controller, for a single-phase VSI with an LC filter. The structure of the control loops, the corresponding modeling procedure and a guideline for the parameter design are explained. The discretization of the control loops understudy is introduced in this chapter. Further, the effectiveness and the robustness of the designed controllers are assessed thought case studies in simulation and experimental setups. The obtained results are presented and discussed in detail showing the performance of the designed controller. The conclusions of this chapter are also drawn.

Chapter IV investigates on proposing a power-sharing control scheme consisting of power calculation and virtual impedance strategies with improved performance for single-phase droop-controlled VSIs in autonomous MG. A brief overview of some methods intended for the power calculation is reported in this chapter. Also, the chapter presents the structure of the proposed scheme incorporating MESOGI-FLL based-power calculation and -virtual impedance control schemes with enhanced performance. The scheme of the power calculation method based on MESOGI-FLL is presented, in which the mathematical analysis of the MESOGI-FLL is developed and its respective model is derived. The performance of this power calculation method compared to the other methods in front of the linear and nonlinear operating condition are discussed. Besides, the structure of the virtual impedance implementation based on the MESOGI-FLL and the analysis of the output impedances are presented. Simulation and experimental case studies are carried out to verify the effectiveness of the proposed power-sharing control based-primary control against nonlinear loads. The obtained results are presented and discussed, confirming the effectiveness of the proposed controller with performance enhancement.

Chapter V summarizes the conclusions of the present thesis. More particular, it presents the description of the proposed control schemes. In addition, the main contributions and outcomes of the thesis are highlighted in this chapter.

1.9 Conclusion

This chapter presents an overview of the microgrid concept, structure and different operating modes is presented. In addition, it provides the description of the hierarchical control of an AC microgrid including primary, secondary, and tertiary control levels. The state of the art regarding the primary control layer and the included control units within is reported. More particular, a review of the droop control methods, power calculation, virtual control strategies and the inner control schemes is provided. Further, the objectives, main contributions and organization of the thesis are given in the present chapter.

In the following chapters, the stated main contributions of the present thesis will be exhibited in details.

Chapter II:

Estimation of the Key Parameters in Single-Phase AC Microgrid System

Chapter II:

Estimation of the Key Parameters in Single-Phase AC Microgrid System

In this chapter, an Enhanced SOGI-FLL scheme suitable for DC-Offset rejection in single-phase microgrid systems is proposed. The proposed scheme can ensure accurate estimation of the required parameters, orthogonal components, frequency, phase, under different disturbances such as DC-offset, phase jump, frequency change, voltage sags and swell.

2.1 Introduction

Microgrids based on renewable energy sources that contain multiple generating units, storage elements, loads and power interfacing converters are seen as a promising architecture in the future distribution network of electric energy [30], [86–88]. Such distributed sources can operate in grid-connected mode, where power quality and current injection are the main tasks of the control loops, and in islanded mode wherein control tasks priority is given to voltage and frequency regulation at the point of common connection (PCC) [89–92]. From this point of view, the concept of a microgrid requires reliable control strategies where safe, stable, and continuous operation is among the most important expectations. To meet the aforementioned requirements, synchronization techniques able to accurately estimate the actual voltage amplitude, operating frequency, and phase at the PCC are the first control stages to be addressed. Phase-locked loops (PLLs) and their derived advanced schemes are the most commonly used techniques for the estimation of the key variables of a given sinusoidal input voltage such as amplitude, phase, and frequency. In single-phase applications, the Second-Order Generalized Integrator-based PLL structure (SOGI-PLL) is the most widely used technique [93, 94]. In this technique, a particular interest is given to the production of accurate two quadrature signals from the sinusoidal input voltage. As an alternative to PLL schemes, Frequency-Locked-Loop (FLL) techniques have gained much more attention in microgrid control applications motivated by the presence of only one loop for frequency estimation instead of two loops in PLL structures [95]. In addition, the FLL-based technique is less sensitive to phase angle jumps which makes it very attractive in such applications. Although this structure has given satisfactory and efficient results in microgrid synchronization, it remains an active research subject especially when

the input voltage is corrupted by harmonics, DC-offset, voltage sags, and swells and frequency and phase variations [96].

The presence of a DC-offset in the measured voltage/current is considered as one of the major issues that affect the proper operation of a microgrid and hence its power quality [97]. In fact, the origin of the DC component comes from two main sources:

i: Drifts in the data acquisition chain caused mainly by imperfections of voltage and current sensors, signal conditioning circuits, and quantification errors in the analog to digital conversion process.

ii: Asymmetry of output waveforms (voltage and current) caused by the disparity of dead times, the disparity of power semi-conductor parameters, and circulating currents between inverters.

Consequently, as the synchronization signal coordinates all the control tasks, the DC component will amplify DC current injection in the main grid, in case of grid-connected mode, and DC voltage when the microgrid operates in islanded mode. It is worth pointing out that DC current injection limits are normalized by the standards IEC61727 [98] and IEEE 1547-2003 [99]. However, the allowed limits of DC-offset in the output voltage are not standardized yet as the concept of microgrids acting as voltage sources are still in research studies and demonstration projects. In the particular case of SOGI-FLL, when the measured input signal is shifted by a DC component results in a remarkable shift of the in-quadrature component and the occurrence of undesirable oscillations in the estimated frequency and phase at the fundamental frequency. Consequently, the removal of these oscillations could be a challenging task due to their low frequency. The aforementioned concerns require particular attention in the design of the synchronization stage and more particularly the ability to reject the DC-offset by an adequate scheme.

Several research papers have addressed the DC-offset rejection in PLL and FLL structures [97], [100–104]. For instance, in [103] SOGI-QSG and SOGI-FLL are used in a cascaded scheme in order to remove the DC-offset superposed to the input voltage. Although this approach has good DC-offset rejection capabilities, it requires high computation time. A similar approach, but with synchronous reference frame PLL is presented in [104]. In reference [105], an adaptive low-pass filter (LPF) is added to the SOGI-FLL structure in order to estimate the input DC-offset. As a result, the input voltage can be cleaned by subtracting the estimated DC component. This scheme also needs an extra computational time due to the adaptive mechanism used to extract the operating frequency. Other similar techniques can be found in [106] and [107].

To cope with this issue, an enhanced second-order generalized integrator-based frequency-locked loop (ESOGI-FLL) intended for DC-offset rejection in both grid-connected and islanded operation of a single-phase voltage source inverter (VSI) is proposed. The proposed scheme aims to estimate accurately the key parameters of the input microgrid voltage and ensure high rejection capabilities of the undesirable effects of the inherent DC-offset superposed to the input microgrid voltage. Unlike the most popular PLLs dealing with DC-offset rejection, the proposed scheme provided low complexity hardware implementation and reduced computation time. In addition, in contrast to other widely used techniques, extra stages are needed to achieve the same objective such as the cascaded structure proposed in [103]. On the other hand, methods based on PLL technique require both stationary reference frame (***αβ***) and synchronous reference frame (***dq***) to handle the DC component. As a result, implementation complexity and extra calculation time are involved. However, the technique suggested in [108] is based only on SOGI-FLL, where its main advantage is the removal of the DC-offset that appears in the estimated orthogonal component. The oscillation in the estimated frequency and phase are not addressed by this technique at all. In order to highlight the effectiveness and robustness of ESOGI-FLL in terms of input voltage parameter estimation, especially in case of high DC-offset value, numerical simulation as well as practical results are reported. The proposed scheme is also tested under corrupted input voltage such as frequency change, phase jump, and voltage sag. Moreover, a detailed comparative study with conventional SOGI-FLL and Third-Order Generalized Integrator-based FLL (TOGI-FLL) presented in reference [108] is reported. The obtained results demonstrate that the proposed ESOGI-FLL has best performances in terms of DC-offset rejection, ripples cancelation in the estimated frequency, and less computational time.

The present chapter is structured as follows; section two gives an overview of the basic structure of SOGI-FLL, where the effect of the DC-offset is highlighted. In section three, the mathematical details of the proposed structure are given. In this section, it is, also, given the DC rejection capabilities and digital implementation of the proposed scheme. Simulation and practical results are reported in sections four and five. Section six presents the conclusion of the present chapter

2.2 Overview of the Basic Structure of SOGI-FLL

In this section, an overview of the basic structure and principle of operation of the SOGI-FLL regarding orthogonal signal generation (OSG) [109], is presented. On the other hand, the main advantages and drawbacks of this method are highlighted particularly in case of the presence of a DC component in the input voltage. The effect of this undesirable component on the frequency-locked loop (FLL) is also presented.

2.2.1 SOGI-QSG

Fig. 2.1 (a) depicts the common structure of SOGI-FLL presented in [109]. The Quadrature Signal Generator (QSG) based on the SOGI scheme, shown in **Fig. 2.1 (b)**, is responsible for generating perfectly filtered direct and orthogonal components, v_α and v_β, respectively. The closed-loop transfer functions G_α and G_β of the output signal components are given by Eq.(2.1) and (2.2), respectively [110].

$$G_\alpha(s) = \frac{v_\alpha(s)}{v(s)} = k\hat{\omega}\frac{s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{2.1}$$

$$G_\beta(s) = \frac{v_\beta(s)}{v(s)} = k\hat{\omega}\frac{\hat{\omega}}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{2.2}$$

Where k stands for a positive adjustable gain chosen as a tradeoff between time response and filtering performances and $\hat{\omega}$ is the estimated frequency obtained in FLL block. This variable must be estimated with a high accuracy which is used to tune the SOGI-QSG adaptive filter.

Bode plots of the closed-loop transfer functions, G_α and G_β, are given in **Fig. 2.2**. Accordingly, it is clearly shown that G_α is a second-order adaptive band-pass filter (ABPF) where the cut-off frequency $\hat{\omega}$ is equal to the input frequency ω. Therefore, the generated voltage v_α and the input voltage v, are in-phase and with the same amplitude. While G_β is a second-order adaptive low-pass filter (ALPF), where at the cut-off frequency $\hat{\omega}$, v_β is in quadrature phase with the input voltage and with the same amplitude as well.

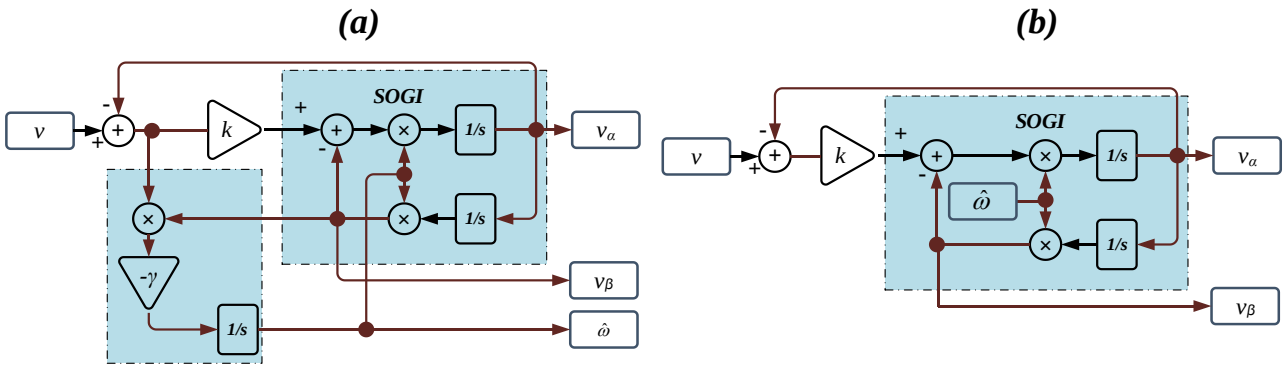


*Fig. 2.1. Common structure of; **(a)** SOGI-FLL, **(b)** SOGI-QSG.*

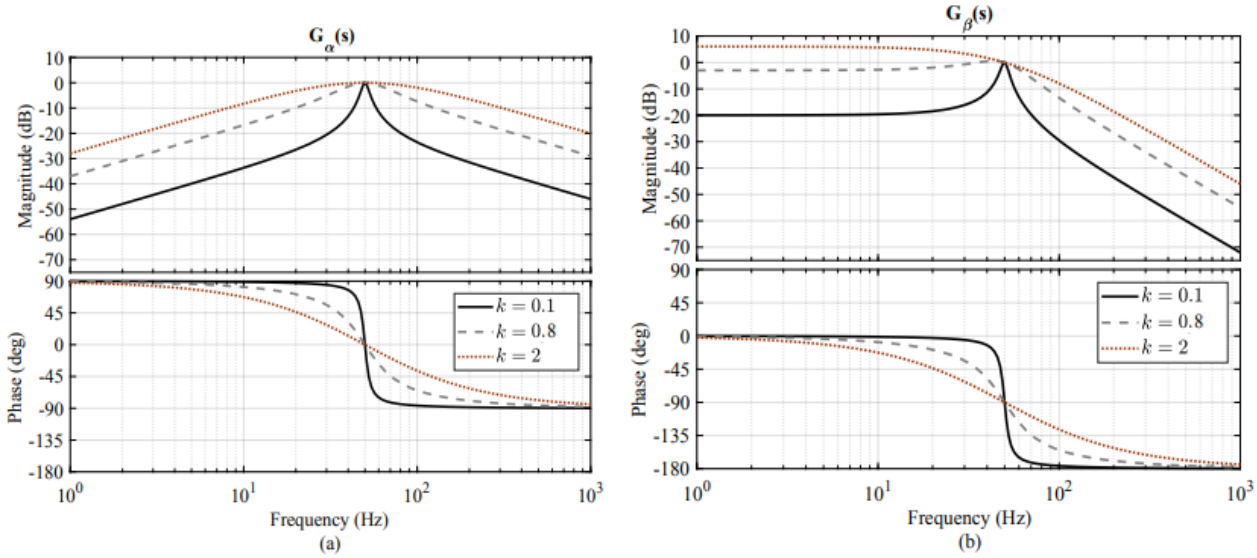


Fig. 2.2. *Bode plots of the closed-loop transfer functions of SOGI-QSG (for* $\hat{\omega}=2\pi\times50$ *rad/s and different values of* k*).*

It is worth pointing out when the input voltage is corrupted by disturbances such as harmonics below the cut-off frequency or a DC-offset, the LPF (G_β) does not reject them sufficiently. As a result, the orthogonal component v_β may contain part of these disturbances and will be shifted by an amount of the input DC-offset.

2.2.2 Frequency-Locked Loop (FLL)

The FLL technique is mainly designed to estimate the input voltage frequency, where SOGI-QSG can be used as a processing block for the adaptive filter [108]. In order to get the desired output voltages, v_α and v_β, in-quadrature phase, and with the same amplitude, the estimated frequency $\hat{\omega}$ of the FLL block, presented in **Fig. 2.3**, should be adapted to the frequency of the input voltage ω. As stated in reference [109], the estimated frequency can be obtained by integrating the product of the difference between the input voltage v and the in-phase component v_α with the orthogonal component v_β as given by the following equation:

$$\hat{\omega} = -\gamma\zeta_f \frac{1}{s} = -\gamma v_\beta (v - v_\alpha)\frac{1}{s} \tag{2.3}$$

where, according to [108], γ is defined as follows:

$$\gamma = \frac{k\hat{\omega}}{V_{\max}^2}\Gamma \tag{2.4}$$

Γ is a positive constant, and V_{max} is the amplitude of the output voltage, given by:

$$V_{\max} = \sqrt{v_\alpha^2 + v_\beta^2}$$

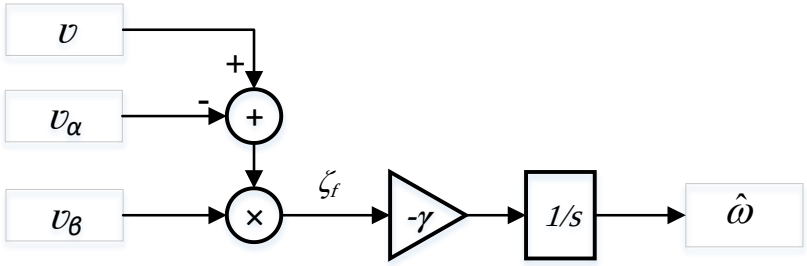


Fig. 2.3. Frequency-Locked Loop (FLL) block diagram.

2.2.3 DC-offset rejection of the conventional SOGI-FLL

This section gives a detailed mathematical analysis showing the DC-offset effects on the orthogonal component v_β and the estimated frequency $\hat{\omega}$ in conventional SOGI-FLL.

These expressions of the transfer function, G_α, and G_β, can be derived in the frequency domain (i.e, $s=j\omega$) as follows:

$$G_\alpha(j\omega)=\frac{jk\hat{\omega}\omega}{\hat{\omega}^2-\omega^2+jk\hat{\omega}\omega} \tag{2.5}$$

$$G_\beta(j\omega)=\frac{k\hat{\omega}^2}{\hat{\omega}^2-\omega^2+jk\hat{\omega}\omega} \tag{2.6}$$

In addition, Eqs. (2.5) and (2.6) can be expressed as a function of their magnitude and phase angle form as given below:

$$G_\alpha(j\omega)=\frac{k\hat{\omega}\omega}{\sqrt{\left(\hat{\omega}^2-\omega^2\right)^2+\left(k\hat{\omega}\omega\right)^2}}\angle\frac{\pi}{2}-\arctan\left(\frac{k\hat{\omega}\omega}{\hat{\omega}^2-\omega^2}\right) \tag{2.7}$$

$$G_\beta(j\omega)=\frac{k\hat{\omega}^2}{\sqrt{\left(\hat{\omega}^2-\omega^2\right)^2+\left(k\hat{\omega}\omega\right)^2}}\angle-\arctan\left(\frac{k\hat{\omega}\omega}{\hat{\omega}^2-\omega^2}\right) \tag{2.8}$$

If assumed an input voltage $v(t)$ with a DC-offset, given by:

$$v(t)=V_{DC}+V_{\max}\sin(\omega t) \tag{2.9}$$

where V_{max}, V_{DC}, and ω are the input voltage amplitude, the added DC-offset, and the input frequency respectively.

The output signals, v_α, and v_β can be expressed in SOGI-QSG as follow:

a- For AC analysis (i. e., V_{DC}**= 0**):

$$v_{\alpha}(t)\Big|_{t\to\infty} = \hat{V}_{\alpha-max}\sin\left(\omega t + \frac{\pi}{2} - \varphi\right) \tag{2.10}$$

$$v_{\beta}(t)\Big|_{t\to\infty} = \hat{V}_{\beta-max}\sin(\omega t - \varphi) \tag{2.11}$$

being $\hat{V}_{\alpha-max}$, $\hat{V}_{\beta-max}$ the magnitudes of the output voltages v_{α} and v_{β}, respectively; φ is the phase angle between the input and the in-phase component. The corresponding expressions can be derived based on frequency domain analysis of the transfer functions G_{α} and G_{β} (Eq. (2.1) and (2.2)). After some mathematical manipulations, $\hat{V}_{\alpha-max}$, $\hat{V}_{\beta-max}$ and φ are given by:

$$\hat{V}_{\alpha-max} = \frac{kV_{max}\hat{\omega}\omega}{\sqrt{\left(\hat{\omega}^2-\omega^2\right)^2 + \left(k\hat{\omega}\omega\right)^2}} \tag{2.12}$$

$$\hat{V}_{\beta-max} = \frac{kV_{max}\hat{\omega}^2}{\sqrt{\left(\hat{\omega}^2-\omega^2\right)^2 + \left(k\hat{\omega}\omega\right)^2}} \tag{2.13}$$

$$\varphi = Arctg\left(\frac{k\hat{\omega}\omega}{\hat{\omega}^2-\omega^2}\right) \tag{2.14}$$

b- For DC analysis (i. e., $v_{AC} = 0$): the expression of v_{α} and v_{β} in steady-state (i. e., $s = 0$) can be obtained as follow:

$$v_{\alpha}(t) = 0 \tag{2.15}$$

$$v_{\beta}(t) = kV_{DC} \tag{2.16}$$

Consequently, the complete form of the output voltages, v_{α}, and v_{β} under frequency-locked condition (i.e., $\hat{\omega} = \omega$) can be expressed as follow:

$$v_{\alpha}(t)\Big|_{\substack{t\to\infty \\ \hat{\omega}\to\omega}} = V_{max}\sin(\omega t) \tag{2.17}$$

$$v_{\beta}(t)\Big|_{\substack{t\to\infty \\ \hat{\omega}\to\omega}} = kV_{DC} - V_{max}\cos(\omega t) \tag{2.18}$$

On the other hand, when substituting Eq. (2.17) and (2.18) into the FLL transfer function (Eq. (2.3)), the resulting ripples in the estimated frequency $\hat{\omega}$ can be derived as follows:

$$\Delta\hat{\omega} = -\gamma k V_{DC}^2 t - \frac{\gamma V_{DC} V_{max}}{\omega}\sin(\omega t) \tag{2.19}$$

From Eq. (2.18), it is clearly shown in SOGI-FLL that the DC-offset still exists in the orthogonal component v_{β}, and its amount depends strongly on the value of k. However, the estimated frequency ripples depend on the added DC-offset as given in Eq. (2.19). This DC value can affect the frequency estimation quality since it may lead to intolerable ripples out of normalized boundaries.

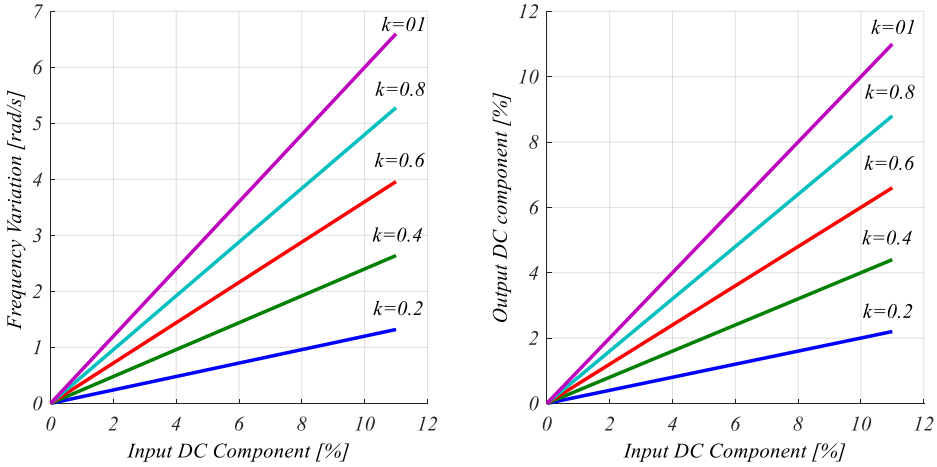


Fig. 2.4. *DC-offset in orthogonal component v_β and amplitude of estimated frequency ripples.*

In order to quantify the DC-offset effect on SOGI-FLL key variables, a simulation study was carried out on the orthogonal component $\boldsymbol{v_\beta}$ and the estimated frequency ripples where the gain $\boldsymbol{k}$ is taken as a sweeping parameter. **Fig. 2.4** shows the amount of DC-offset in $\boldsymbol{v_\beta}$ and ripples amplitude variation as a function of the added DC-offset in the input voltage for different values of $\boldsymbol{k}$.

2.3 Proposed Enhanced SOGI-FLL Scheme

In this section, an enhanced structure intended for DC-offset rejection in the orthogonal component $\boldsymbol{v_\beta}$ and ripples cancelation in the estimated frequency $\boldsymbol{\hat{\omega}}$ is presented. Actually, this approach is an alternative to tackle the above-mentioned drawbacks of conventional SOGI-FLL

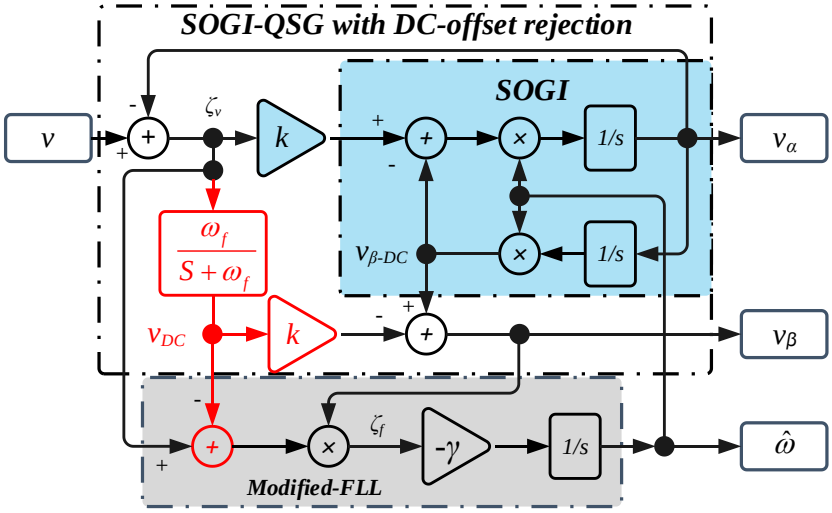


Fig. 2.5. *The Enhanced SOGI-FLL (ESOGI-FLL) structure.*

The proposed ESOGI-FLL, shown in

Fig. 2.5, consists of two main blocks: SOGI-OSG block including offset rejection proposed in [100], and a modified frequency-locked loop block.

2.3.1. SOGI-QSG with offset rejection

To overcome the weakness of the conventional SOGI-QSG scheme to reject sub-harmonics and cancel DC-offset, an improved SOGI-QSG including offset rejection is proposed in [100]. The block diagram depicted in **Fig. 2.6** shows the main differences between the conventional SOGI-QSG and SOGI-QSG including offset rejection structure. As shown in **Fig. 2.3**, an additional low-pass filter (LPF) with a fixed cut-off frequency ω_f is included in the SOGI-QSG structure in order to estimate the DC component that might exist in the input voltage. Thus, the required orthogonal component (i.e., v_β) is generated by subtracting the original quadrature signal $v_{\beta\text{-}DC}$ obtained by the conventional SOGI-QSG structure and the output of the added LPF (v_{DC}). Therefore, the DC-offset and sub-harmonics contained in the input voltage are effectively removed from the generated v_β. The new quadrature signal v_β is calculated using the following equation:

$$v_\beta = v_{\beta-DC} - k v_{DC} \tag{2.20}$$

According to the structure given in **Fig. 2.6**, the closed-loop transfer functions of the generated voltages (v_α, v_β, and v_{DC}) are given by the following expressions:

$$G_\alpha(s) = \frac{v_\alpha(s)}{v(s)} = k\hat{\omega}\frac{s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{2.21}$$

$$G_\beta(s) = \frac{v_\beta(s)}{v(s)} = \frac{k\left(\hat{\omega}^2 - \omega_f s\right)}{s + \omega_f}\frac{s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{2.22}$$

$$G_{v_{DC}}(s) = \frac{v_{DC}(s)}{v(s) - v_\alpha(s)} = \frac{\omega_f}{s + \omega_f} \tag{2.23}$$

The gain and phase plots of G_α and G_β are given in **Fig. 2.7 (a)** and **(b)**, respectively. According to these plots, one can notice the bandpass filtering features for both of them and then a good DC-offset rejection can be achieved. The selection of the LPF cutoff frequency "ω_f" is carried out as a tradeoff between the desired transient response of the frequency estimate and acceptable harmonic rejection (sub-harmonics and high harmonics) of the orthogonal component v_β. In **Fig. 2.7 (b)** and **(c)**, it is shown the bode plot of the transfer function, G_β, and the transient response of the frequency estimate corresponding to three different values of the LPF frequency ω_f.

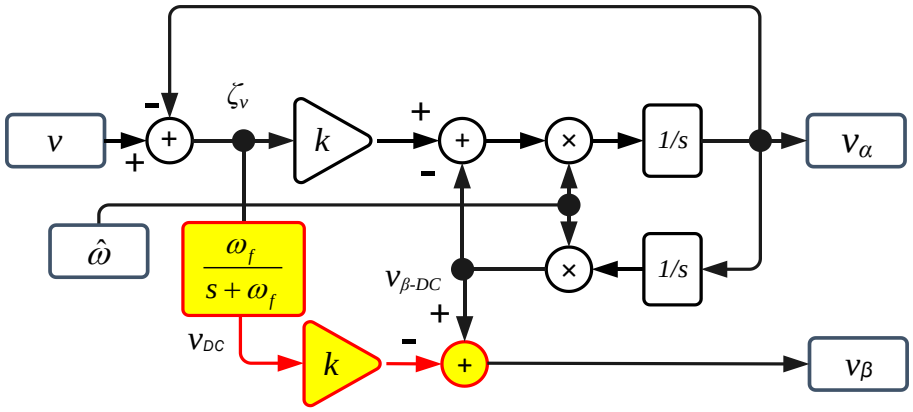


Fig. 2.6. *SOGI-QSG with Offset rejection structure*

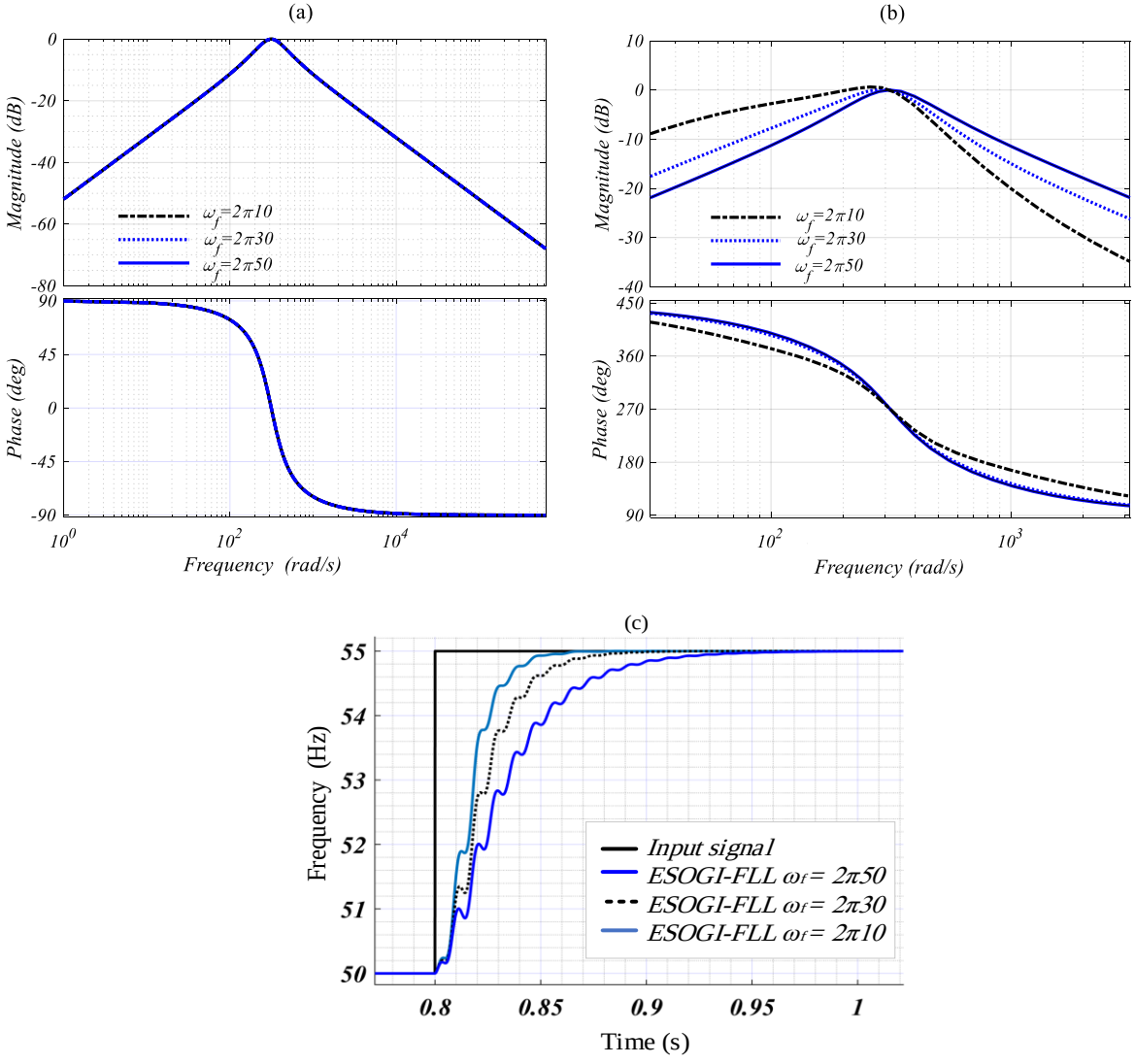


Fig. 2.7. *Bode plots of the transfer functions:* ***(a)*** G_α *and* ***(b)*** G_β*, and* ***(c)*** *the frequency estimate for different values of cut-off frequency* ω_f*.*

From these figures, it is clearly shown that a high value of ω_f can ensure good rejection of sub-harmonics, but on the other hand, slows-down the transient response of the frequency estimate, and vice versa. Hence, in our proposal, the LPF frequency is chosen to be 30 Hz.

2.3.2. The proposed modified FLL block

In order to enhance the quality of the estimated frequency, in terms of cancelation of ripples which are highly dependent on the DC-offset value, an enhanced FLL block is designed to eliminate these ripples. The modification brought for this block is shown in **Fig. 2.8**. The main idea behind this modification is to eliminate the DC component v_{DC} by subtracting it from the error voltage ζ_v. Accordingly, the estimated frequency $\hat{\omega}$ is then obtained by the following expression:

$$\hat{\omega} = -\frac{\gamma}{s} v_\beta \left(v - v_\alpha - v_{DC} \right) \tag{2.24}$$

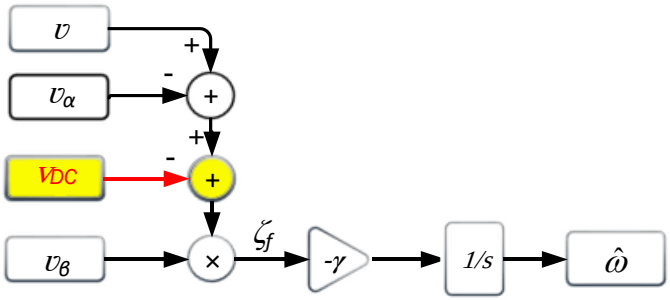


Fig. 2.8. Proposed modified FLL block.

2.3.3. DC-offset Rejection of The Proposed scheme

Hereafter the detailed demonstration of the DC-Offset rejection by the proposed ESOGI-FLL structure is given. In particular, DC rejection from vβ and ripples elimination from the estimated frequency are highlighted. To this end, let us assume that the input voltage v(t) is the same as given in **Eq. (2.9)**. Therefore, the steady-state of the ESOGI-OSG outputs, v_α, v_β, and v_{DC} are given by:

$$v_\alpha(t)\big|_{t\to\infty} = \hat{V}_{\alpha-max} \sin\left(\omega t + \frac{\pi}{2} - \varphi\right) \tag{2.25}$$

$$v_\beta(t)\big|_{t\to\infty} = kV_{DC} + \hat{V}_{\beta-max} \sin(\omega t - \varphi) - kv_{DC}(t) \tag{2.26}$$

$$v_{DC}(t) = V_{DC} + \frac{\omega_f}{\sqrt{\omega_f{}^2 + \omega^2}} \left(V_{max} \sin(\omega t) - V_{\alpha-max} \sin\left(\omega t + \frac{\pi}{2} - \varphi\right) \right) \tag{2.27}$$

Under frequency-locked condition (i.e., $\hat{\omega} = \omega$) and based on **Eqs. (2.12), (2.13)** and **(2.14)**,

equations **(2.25), (2.26)**, and **(2.27)** yield to:

$$v_\alpha(t)\Big|_{\substack{t\to\infty \\ \hat{\omega}\to\omega}} = V_{max}\sin(\omega t) \tag{2.28}$$

$$v_\beta(t)\Big|_{\substack{t\to\infty \\ \hat{\omega}\to\omega}} = -V_{max}\cos(\omega t) \tag{2.29}$$

$$v_{DC}(t) = V_{DC} \tag{2.30}$$

Substituting **Eq. (2.28), (2.29)** and **(2.30)** in **Eq. (2.24)**, the estimated frequency ripples become:

$$\Delta\hat{\omega} = 0 \tag{2.31}$$

Therefore, the proposed ESOGI-FLL structure can effectively eliminate the DC-offset in v_β, and then the estimated frequency is ripples free.

2.4 Stability analysis of the proposed scheme

In order to prove the convergence of the proposed scheme, the stability analysis based on Lyapunov nonlinear method is performed.

Based on the transfer function of v_α, v_β, and the DC-Offset output of LPF filter given by **Eqs. (2.21), (2.22)** and **(2.23)** respectively, one can derive the state-space equations as follows:

$$\dot{x} = \begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = Ax + Bv = \begin{bmatrix} 0 & 1 & 0 \\ -\hat{\omega}^2 & -k\hat{\omega} & 0 \\ 0 & -\omega_f & -\omega_f \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ k\hat{\omega} \\ \omega_f \end{bmatrix}[v] \tag{2.32}$$

$$y = \begin{bmatrix} v_\alpha \\ v_{\beta-DC} \\ v_{DC} \end{bmatrix} = Cx = \begin{bmatrix} 0 & 1 & 0 \\ \hat{\omega} & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} \tag{2.33}$$

$$\dot{\hat{\omega}} = -\gamma(\hat{\omega}x_1 - kx_3)(v - x_2 - x_3) \tag{2.34}$$

where $\boldsymbol{x}$ and $\boldsymbol{y}$ denote the state and the output vectors, respectively, and $\dot{\hat{\omega}}$ is the first derivative of the estimated frequency.

For a complex input voltage consisting of an AC-component and DC-component, a superposition method is applied to analyses the output vector in steady-state. Hence, for a given input voltage $v = v_{DC} + v_{AC}$, the state vector x and the output vector y can be written as follows:

$$\begin{cases} x = x_{DC} + x_{AC} \\ y = y_{DC} + y_{AC} \end{cases} \tag{2.35}$$

where $v_{DC/AC}$, $x_{DC/AC}$ and $y_{DC/AC}$ are the input voltage, the state vector and the output vector DC and AC components, respectively.

By substituting **Eq. (2.35)** in **Eq. (2.33)** and **Eq. (2.34)** the following state-space equations, in steady state, can be derived:

a- In case of DC analysis: (i.e., $v_{DC} = V_{DC}$, $v_{AC} = 0$)

$$\dot{\bar{x}}_{DC} = \begin{bmatrix} \dot{\bar{x}}_{1-DC} \\ \dot{\bar{x}}_{2-DC} \\ \dot{\bar{x}}_{3-DC} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{2.36}$$

$$\bar{x}_{DC} = \begin{bmatrix} \bar{x}_{1-DC} \\ \bar{x}_{2-DC} \\ \bar{x}_{3-DC} \end{bmatrix} = \begin{bmatrix} \frac{k}{\hat{\omega}} V_{DC} \\ 0 \\ V_{DC} \end{bmatrix} \tag{2.37}$$

$$\bar{y}_{DC} = \begin{bmatrix} \bar{v}_{\alpha-DC} \\ \bar{v}_{\beta-DC-DC} \\ \bar{v}_{DC-DC} \end{bmatrix} = \begin{bmatrix} 0 \\ kV_{DC} \\ V_{DC} \end{bmatrix} \tag{2.38}$$

where V_{DC} is the DC-offset componenet of the input voltage.

b- In case of AC analysis: (i.e., $v_{DC} = 0$, $v_{AC} = V_{Max}\sin(\omega t+\varphi)$) and by disabling the frequency estimation loop (i.e., $\hat{\omega} = 0$), the following to case are considered:

b. 1. If $\hat{\omega} = \omega$ (i.e., under stable operating condition), the state and the output vectors can be obtained as follow:

$$\dot{\bar{x}}_{AC} = \begin{bmatrix} \dot{\bar{x}}_{1-AC} \\ \dot{\bar{x}}_{2-AC} \\ \dot{\bar{x}}_{3-AC} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -\omega^2 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \bar{x}_{1-AC} \\ \bar{x}_{2-AC} \\ \bar{x}_{3-AC} \end{bmatrix} \tag{2.39}$$

$$\bar{x}_{AC} = \begin{bmatrix} \bar{x}_{1-AC} \\ \bar{x}_{2-AC} \\ \bar{x}_{3-AC} \end{bmatrix} = \begin{bmatrix} \bar{x}_{1-AC} \\ v_{AC} \\ 0 \end{bmatrix} \tag{2.40}$$

$$\bar{y}_{AC} = \begin{bmatrix} \bar{v}_{\alpha-AC} \\ \bar{v}_{\beta-DC-AC} \\ \bar{v}_{DC-AC} \end{bmatrix} = \begin{bmatrix} \bar{x}_{2-AC} \\ \omega\bar{x}_{1-AC} \\ 0 \end{bmatrix} = \begin{bmatrix} V_{max}\sin(\omega t+\varphi) \\ -V_{max}\cos(\omega t+\varphi) \\ 0 \end{bmatrix} \quad (2.41)$$

where V_{max} is the magnitude of the input voltage and ($\bar{}$) stands for the steady-state condition.

b. 2. If $\hat{\omega} \neq \omega$, the expression of the output vector can be obtained as:

$$\bar{y}_{AC} = \begin{bmatrix} \bar{v}_{\alpha-AC} \\ \bar{v}_{\beta-AC} \\ \bar{v}_{DC-AC} \end{bmatrix} = \begin{bmatrix} V_{\alpha-max}\sin(\omega t+\varphi-\phi) \\ -V_{\beta-max}\cos(\omega t+\varphi-\phi) \\ \dfrac{\omega}{\sqrt{\omega_f^2+\omega^2}}\left(v_{AC}-\bar{v}_{\alpha-AC}\right) \end{bmatrix} \quad (2.42)$$

where $V_{\alpha-max}$, $V_{\beta-max}$ and ϕ are defined by **Eqs. (2.14), (2.15)** and **(2.16)** given above.

As it can be observed from **Eqs. (2.42)** and **(2.43)**, when the frequency estimation loop is disabled, the output vector still kept its stable sinusoidal waveforms.

Regarding the modified FLL stability, when a sinusoidal input voltage at the frequency ω is taken as an input for SOGI-FLL and considering a small error between the estimated frequency and the input one, according to **Eq. (2.44)**, the following steady-state relationship of the states can be approximated similarly as **Eq. (2.40)** [100]:

$$\begin{cases} \dot{\bar{x}}_{2-AC} = -\omega^2\bar{x}_{1-AC} \\ \bar{x}_{3-AC} = 0 \end{cases} \quad (2.43)$$

Therefore, the frequency error in steady-state can be written according to **Eq. (2.41)** and **Eq. (2.38)** as follows:

$$\bar{\zeta}_f = \left(\hat{\omega}x_1 - kx_3\right)\left(\bar{v}-\bar{x}_2-\bar{x}_3\right) = \left(\hat{\omega}\left(\bar{x}_{1-DC}+\bar{x}_{1-AC}\right)-k\left(\bar{x}_{3-DC}+\bar{x}_{3-AC}\right)\right)\left(\bar{v}_{DC}-\bar{x}_{2-DC}-\bar{x}_{3-DC}+\bar{v}_{AC}-\bar{x}_{2-AC}-\bar{x}_{3-AC}\right) \quad (2.44)$$

In addition, from **Eqs. (2.36) to (2.38)** and **Eq. (2.42), Eq. (2.45)** becomes:

$$\bar{\zeta}_f = \left(\hat{\omega}\bar{x}_1 - k\bar{x}_3\right)\left(\bar{v}-\bar{x}_2-\bar{x}_3\right) = \hat{\omega}\bar{x}_{1-AC}\left(\bar{v}_{AC}-\bar{x}_{2-AC}\right) \quad (2.45)$$

Accordingly, from **Eqs. (2.32), (2.44)** and **(2.46)**, the frequency error in steady-state can be expressed by:

$$\bar{\zeta}_f = \frac{\bar{x}_{1-AC}}{k}\left(\dot{\bar{x}}_{2-AC}+\hat{\omega}^2\bar{x}_{1-AC}\right) = \frac{\left(\bar{x}_{2-AC}\right)^2}{k}\left(\hat{\omega}^2-\omega^2\right) \quad (2.46)$$

This expression denotes that the term ζ_f collects information about the error in frequency

estimation and, hence, it is suitable to act as the control signal of the FLL block. An analysis of the local stability of the FLL can be conducted by considering $\hat{\omega} \approx \omega$. In such a case, the term $\hat{\omega}^2 - \omega^2$ can be approximated as $2\omega(\hat{\omega} - \omega)$, then, the local dynamics of the FLL can be described by:

$$\dot{\hat{\omega}} = -\gamma \bar{\zeta}_v \approx -\gamma \frac{2\hat{\omega}\bar{x}_{2-AC}^2}{k}\left(\hat{\omega} - \omega\right) \tag{2.47}$$

Defining the error in frequency estimation as $\delta = (\hat{\omega} - \omega)$ its derivative is given by $\dot{\delta} = (\dot{\hat{\omega}})$ (where ω is considered as constant). Therefore, the given statement for **Eq. (49)** will be always true for positive values of $\hat{\omega}$. This condition is the key for the local stabilization mechanism of the FLL.

$$\dot{\delta}\delta = -\gamma \frac{2\hat{\omega}\bar{x}_{2-AC}^2}{k}\delta^2 \leq 0 \tag{2.48}$$

Accordingly, the convergence of the proposed scheme is guaranteed. This refers to that in steady-state, the DC component is totally rejected from the inputs of the FLL estimator. So, the stability of the proposed FLL scheme is not influenced by the DC-offset estimation block.

2.5 Digital Implementation and Computation Burden

The digital implementation of the proposed ESOGI-QSG is carried out by discretizing **Eqs. (2.21)** to **(2.23)**, by using trapezoidal integration method. The corresponding block diagram of the SOGI-FLL in discrete representation is shown in **Fig. 2.9**. According this figure the discrete mathematical forms of the SOGI-FLL outputs are derived as:

$$\begin{cases} v_\alpha(k) = x(k) - x(k-2) \\ v_{\beta-DC}(k) = \dfrac{T_s\hat{\omega}}{2}\left(x(k) + 2x(k-1) + x(k-2)\right) \\ v_{DC}(k) = r(k) + r(k-1) \end{cases} \tag{2.49}$$

where T_s is the sampling time, ***x(n)***, and ***r(n)*** are internal states. They can be expressed as follow:

$$x(k) = b_0 v(k) - a_0 x(k-1) - a_1 x(k-2) \tag{2.50}$$

$$r(k) = a_2 r(k-1) + b_1\left(v(k) - v_\alpha(k)\right) \tag{2.51}$$

The parameters a_0, a_1, a_2, b_0, and b_1 are given by:

$$\begin{cases} a_0 = \left[\dfrac{2\hat{\omega}^2T_s^2 - 8}{4 + 2kT_s\hat{\omega} + \hat{\omega}^2T_s^2}\right], a_1 = \left[\dfrac{4 - 2kT_s\hat{\omega} + \hat{\omega}^2T_s^2}{4 + 2kT_s\hat{\omega} + \hat{\omega}^2T_s^2}\right], a_2 = \dfrac{2 - T_s\omega_f}{2 + T_s\omega_f}, \\ b_0 = \dfrac{2kT_s\hat{\omega}}{4 + 2kT_s\hat{\omega} + \hat{\omega}^2T_s^2}, \quad b_1 = \dfrac{T_s\omega_f}{2 + T_s\omega_f} \end{cases} \tag{2.52}$$

In order to evaluate the computation burden and its comparison with conventional SOGI-FLL and TOGI-FLL, shown in **Fig. 2.9**, an in-depth investigation on the required number of mathematical operations of each of them is performed and the main results are summarized in **Table 2.1.**

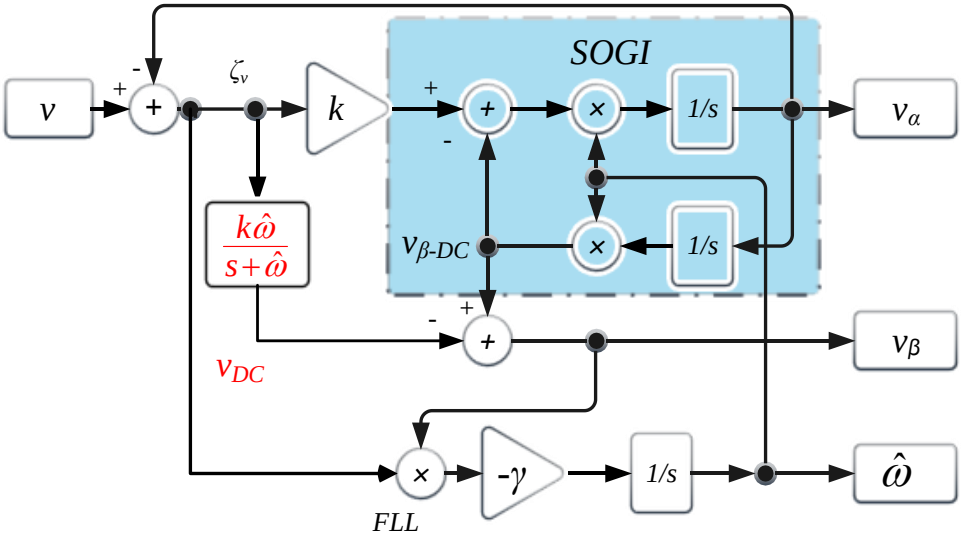


Fig. 2.9. *The TOGI-FLL structure [79].*

Table 2.1. *NUMBER OF OPERATIONS PERFORMED BY EACH METHOD : M = MULTIPLICATION (1 CYCLE), A = ADDITION (1 CYCLE), D = DIVISION (14 CYCLE) AND S = VARIABLE STORAGE (4 CYCLE), FOR SINGLE PRECISION, FLOATING POINT NUMBERS IN STM CORTEX4 [109].*

Structure	*M*	*A*	*D*	*S*	*Number of Cycle*
SOGI-FLL	17	15	5	3	114
TOGI-FLL	19	20	7	4	153
ESOGI-FLL	20	19	5	4	125

As can be seen, conventional SOGI-FLL takes the smallest number of the required mathematical operations, whereas in ESOGI-FLL the number of involved mathematical operations is slightly greater than conventional SOGI-FLL and less than TOGI-FLL. Although this minor additional operation in comparison with conventional SOGI-FLL, the brought performances are highly superior regarding DC-offset rejection and frequency ripples cancelation. In addition, there are only 11 additional cycles needed to perform ESOGI-FLL when compared to the conventional SOGI-FLL

method, which can be considered not significant with regard to the obtained advantages.

2.6 Simulation results and discussion

A simulation study is carried out as case studies to assess the effectiveness of the proposed ESOGI-FLL in terms of DC-offset rejection and frequency ripples cancelation. Towards this end, the DC-offset value —with variable level taken as a percentage of the input voltage amplitude— is added to the input voltage. The behavior of ESOGI-FLL outputs for common disturbances such as frequency change, phase jump, and voltage sag are also simulated and compared to SOGI-FLL and TOGI-FLL performances. The main parameters taken for the simulation study are given in ***Table 2.2*** and ***Table 2.3***, given bellow.

Table 2.2. *PARAMETERS OF THE INVERTER POWER STAGE*

Parameter	Symbol	Unit	Value
Nominal Voltage	V_{max}	V	310
Nominal frequency	$\omega / 2\pi$	Hz	50
Switching frequency	f_s	kHz	20
DC bus voltage	U_{dc}	V	450
Loads	R_L	Ω	60
Filter Capacitor	C_f	µF	10
Filter inductor	L_f	mH	0.1

Table 2.3. *FLL PARAMETERS*

Parameter	Symbol	Unit	Value
SOGI-QSG gain	k	-	0.8
FLL gain	Γ	s^{-1}	50
LPF cut-off frequency	$\omega_f / 2\pi$	Hz	30

a) Case 1: DC-offset Rejection Assessment

In this simulation study, a step change of DC-offset is superposed to the input voltage. In the first test, a step change of DC-offset from 5% to 10% and in the second one from **5%** to **100%** and both of them occur at **t = 0.2s**. Simulation results, showing the time evolution of orthogonal component $\boldsymbol{v_\beta}$, estimated frequency, and phase error for both tests, are depicted in **Fig. 2.10** and **Fig. 2.11** respectively.

According to these results, one can note that with a moderate DC-offset, (**5%** to **10%**), the orthogonal component $\boldsymbol{v_\beta}$ is accurately estimated in both ESOGI-FLL and TOGI-FLL, while the obtained by the conventional SOGI-FLL is slightly shifted with a residual DC-offset (**Fig. 2.10**. **a**).

However, remarkable ripples in steady-state still exist in the estimated frequency and phase error, obtained by conventional SOGI-FLL and TOGI-FLL methods. But in the case of the proposed ESOGI-FLL scheme, the estimated frequency and phase error are ripple-free, as clearly shown in **Fig. 2.10 (b)** and **(c)**. **Fig. 2.11**, presents the obtained results for the same variables when a **100%** DC-offset is added to the input voltage at **t = 0.2s**. In this test, SOGI-FLL completely fails to estimate the whole variables (i.e. $\boldsymbol{v_{\beta}}$, $\hat{\omega}$, $\boldsymbol{\delta\varphi}$) while TOGI-FLL gives a distorted orthogonal component and a wrong estimation of both frequency and phase error. However, with the proposed method, the orthogonal component v_{β}, and the estimated frequency and phase error are still unchanged despite the amount of the introduced DC component in the input voltage.

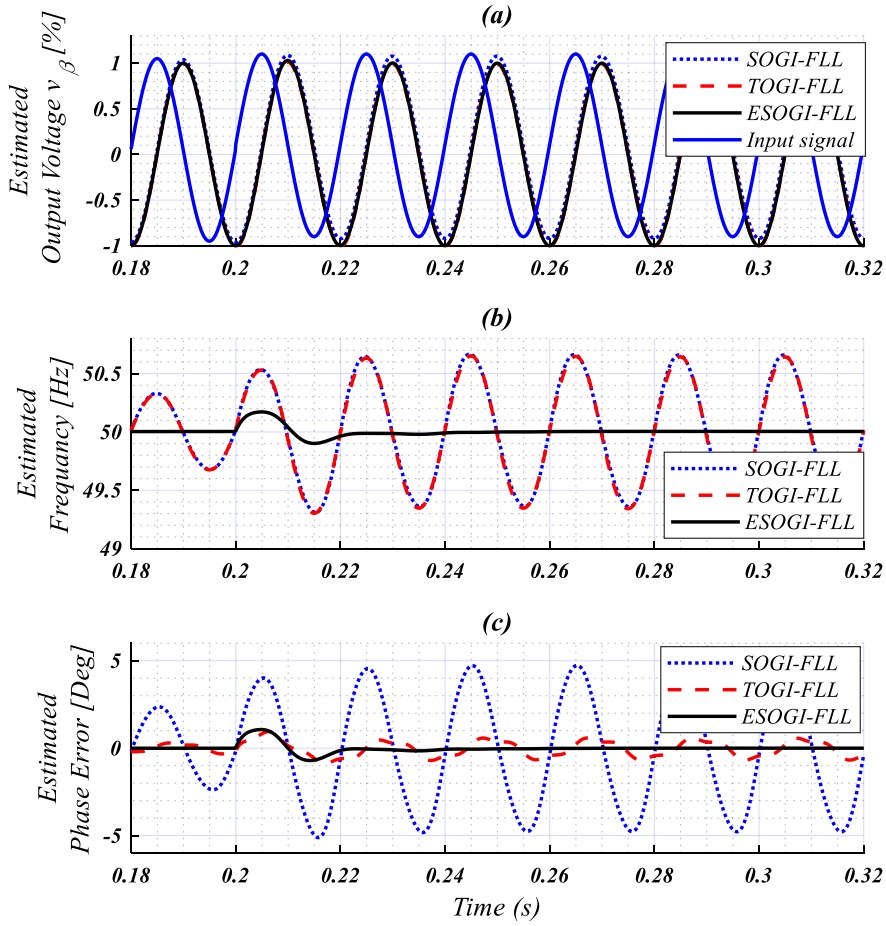


Fig. 2.10. *Output voltage v_{β}, estimated frequency and phase error in the case of 10% DC-offset.*

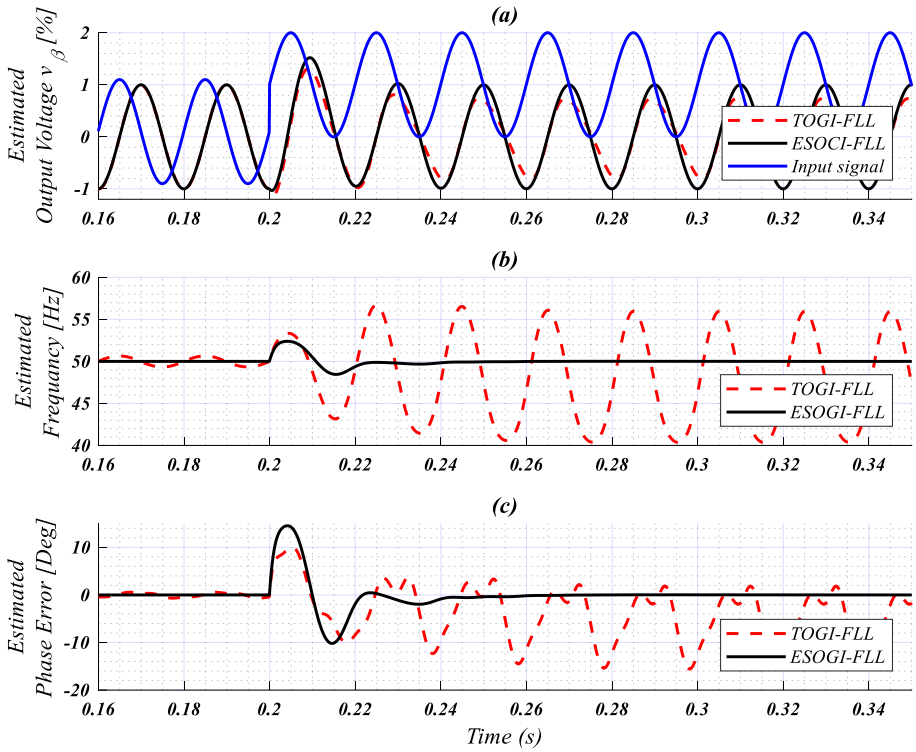


Fig. 2.11. *Output voltage vβ, estimated frequency and phase error in the case of 100% DC-offset.*

b) Case 2: Frequency change and phase jump assessment

In this case study, ESOGI-FLL is tested against frequency change and phase jump introduced in the input voltage and containing 10% DC-offset to assess its performances in terms of tracking and frequency-locked loop performances. Towards this end, a ramp change in the input frequency, from **50** to **55 Hz**, is simulated. The results shown in **Fig. 2.12 (a)** and **(b)**, depict the time evolution of the estimated frequency and phase error versus those obtained by SOGI-FLL and TOGI-FLL.

It is clearly shown that the estimated variables, frequency, and phase error, obtained by the ESOGI-FLL method tend steadily toward the reference frequency and phase error without ripples. Regarding the settling time, which is of prime interest in the synchronization issue, it is found to be the same as given by SOGI-FLL and TOGI-FLL (t_s **= 50 ms**).

Simulation results for the phase change scenario, with the same rate of DC-offset injection, are given in **Fig. 2.13 (a)** and **(b)**. The test is carried out with a phase jump of 20° in the input signal. The same results for the estimated frequency and phase error as in the first test are presented. However, the settling time has slightly increased relative to the first test (t_s **= 70 ms**).

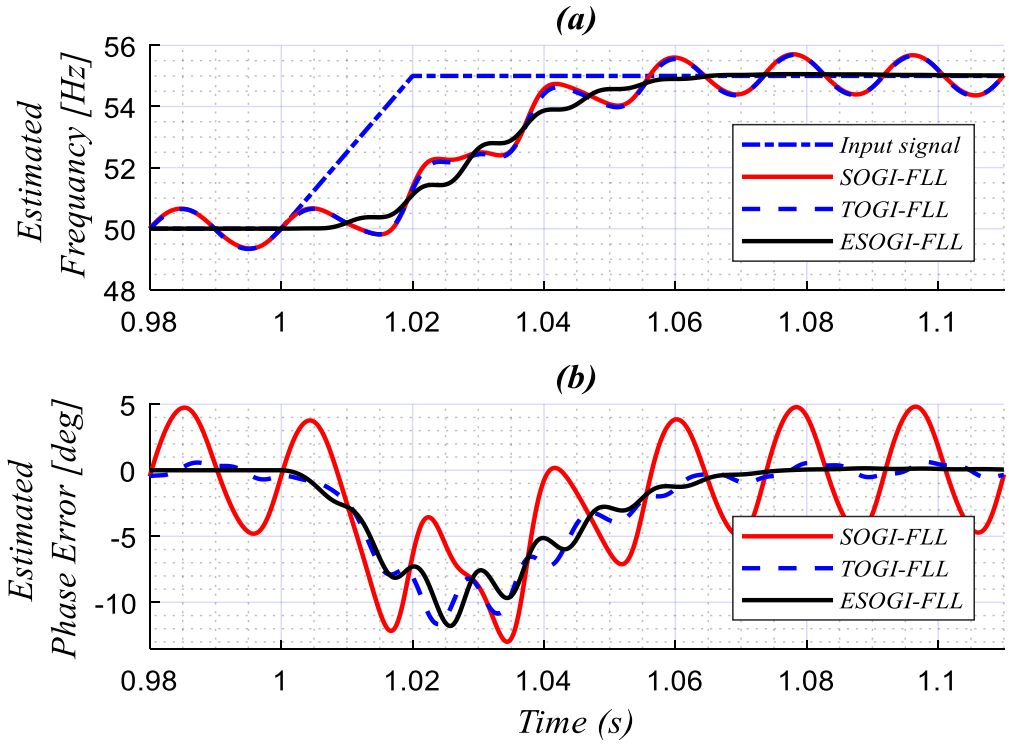


Fig. 2.12. *Estimated frequency and phase error in case of frequency change.*

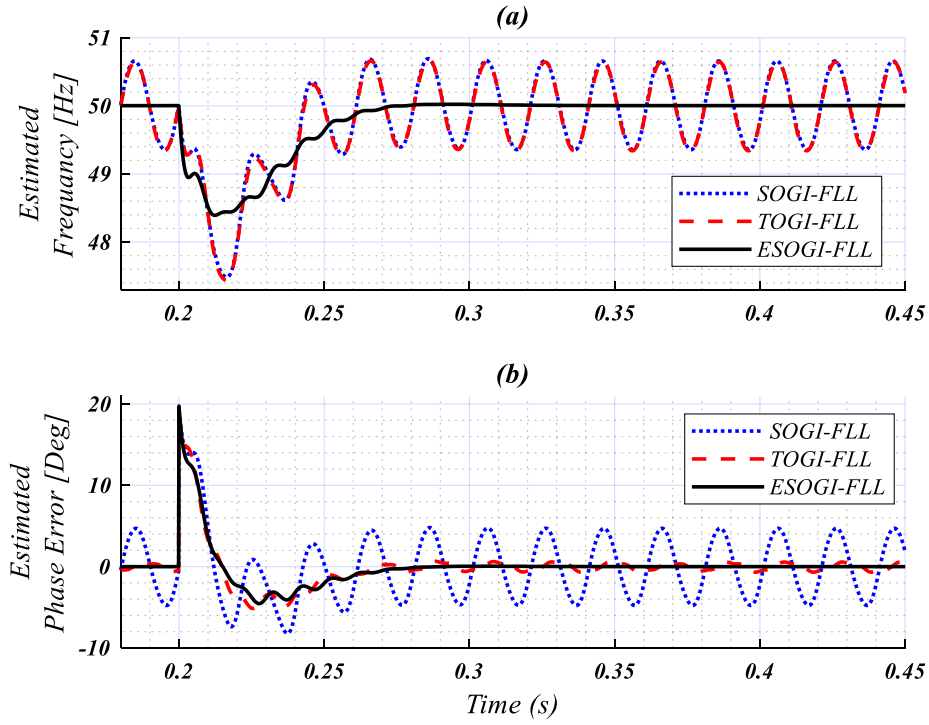


Fig. 2.13. *Estimated frequency and phase error in case of phase jump.*

c) Case 3: Sag test assessment

In this test, a sudden sag, with a reduction of **50%** of the input voltage amplitude and time duration of **0.1s**, is introduced deliberately at **t = 1s**. The corresponding simulation results are shown in **Fig. 2.14 (a), (b)** and **(c)**. As it can be seen, ESOGI-FLL provides smooth responses of the estimated frequency and phase error.

d) Case 4: Harmonics rejection test assessment

In this case, the effectiveness of the proposed scheme for the estimation of the key MG parameters in the case of highly distorted AC voltage is demonstrated. Thus, a simulation study is carried out where the AC voltage is altered by harmonics (**H3, H5**, and **H7**). The amplitude amount of the aforementioned harmonics is listed hereafter:

- **H3**: **30%** from the fundamental input signal
- **H5**: **10%** from the fundamental input signal
- **H7** : **08%** from the fundamental input signal
- DC-offset: **10%** to **100%** (at **t = 0.2s**) from the fundamental input signal.

The obtained results of both the proposed scheme and the TOGI-FLL scheme for this case study are illustrated in **Fig. 2.15**. From this figure, one can be seen that the proposed scheme extracted properly filtered orthogonal components and reject totally the injected harmonics. In addition, it can be observed that the proposed scheme estimates accurately the microgrid frequency without any ripples, while, there are noticeable ripples occur in the estimated frequency by the TOGI-FLL scheme. Regarding the phase angle estimation, both schemes extract this parameter properly. It is worth mentioning that the THD injected harmonics in the input voltage is **32.62%**, where the THD of estimated direct component v_α is **3.46%**. The obtained results showed the effectiveness of the proposed scheme even in case of a high distorted input voltage.

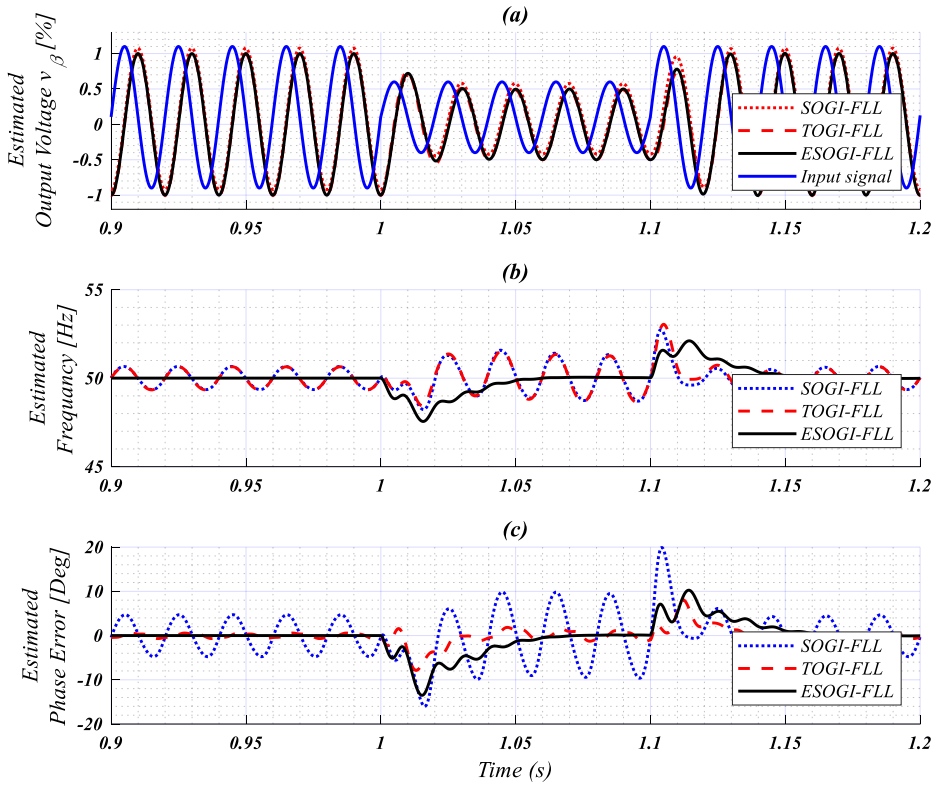


Fig. 2.14. *Output signal* v_β*, estimated frequency, and phase error in case 3.*

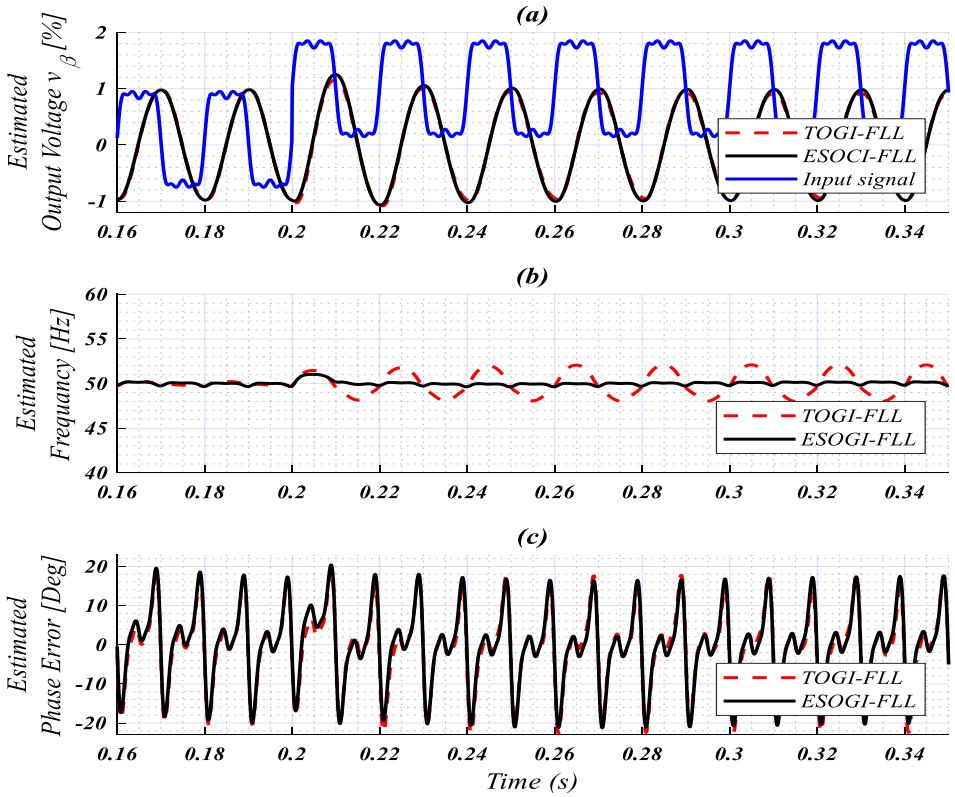


Fig. 2.15*. Estimated parameters in the case of the 3, 5, and 7 harmonics injection.*

2.7 Experimental results

In order to experimentally confirm the previous theoretical and simulation results, the circuit diagram shown in **Fig. 2.16** is configured to implement the proposed approach. Actually, the experimental setup consists of a single-phase PWM H-bridge inverter with an LC filter feeding a resistive load. This inverter can be considered as an emulated AC source where the reference voltage is altered intentionally to produce the desired distorted voltage at the output terminals. These disturbances can practically take place in transformer-less PV grid-connected system or AC islanded microgrid, such as DC-offset, frequency change, phase jump, sags and swells. Then, the output voltage is sensed and entered into the proposed ESOGI-FLL scheme; implemented in and **ARM Cortex-M4** microcontroller (**STM32F407ZG** board); in order to compute the desired parameters. The parameters taken for this experimental setup are the same as those set in ***Table 2.2*** and ***Table 2.3***.

Experimental results shown in **Figs. Fig. 2.17**, **Fig. 2.18**, **Fig. 2.19** and **Fig. 2.20**, depict experimental results corresponding to: i): DC-offset variation from **0%** to **50%** (**Fig. 2.17**); ii): Frequency ramp change from **50 Hz** to **55 Hz** (**Fig. 2.18**); iii): Phase jump of **30°** (**Fig. 2.19**), iv): Voltage sag of **30%** (**Fig. 2.20**). It is clearly shown the effectiveness of the proposed method to estimate accurately the key parameters without shifts and ripples.

A detailed comparison of the proposed method with SOGI-FLL and TOGI-FLL, in terms of estimated frequency value, ripples amplitude, and v_β DC-offset percentage, has been carried out focusing on theatrical and simulation study as well as practical results. ***Table 2.4*** summarizes these findings for a DC-offset up to **100%** of the input signal amplitude.

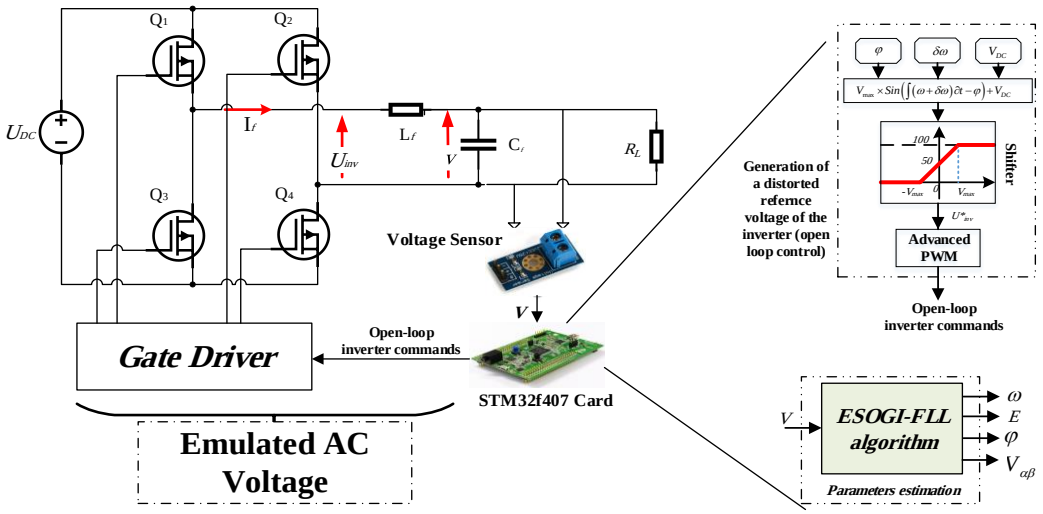


Fig. 2.16. Block diagram of the setup test procedure of ESOGI-FLL performances.

Regarding these results, it is worth pointing out the following points:

- The proposed ESOGI-FLL allows total DC-offset rejection even in the worst case when DC-offset reaches **100%** of the input signal amplitude.
- The estimated frequency is ripples free using the ESOGI-FLL method.
- SOGI-FLL fails in estimating the input signal parameters when the DC-offset reaches 12%.
- TOGI-FLL has the same performances as ESOGI-FLL regarding DC-offset rejection.
- Nevertheless, when DC-offset is quiet high, it fails to estimate the frequency.

These results prove that the proposed ESOGI-FLL has better performances, especially when a significant value of DC-offset is introduced into the input signal.

Table 2.4. *COMPARATIVE STUDY BETWEEN SOGI-FLL, TOGI-FLL, AND ESOGI-FLL*

Parameter / *Technique*	*Input DC-Offset (%)*	*Estimated frequency (Hz)*		*Frequency ripples amplitude (Hz)*			*V_β DC-Offset (%)*		
		Simulation	*Practical*	*Theoretical*	*Simulation*	*Practical*	*Theoretical*	*Simulation*	*Practical*
SOGI-FLL	*0.55*	*49.98*	*49.98*	*0.042*	*0.03*	*0.03*	*0.44*	*0.33*	*0.33*
TOGI-FLL	*0.33*	*49.99*	*49.98*	*0.025*	*0.052*	*0.043*	*0*	*0.04*	*0.06*
ESOGI-FLL	*0.89*	*50*	*50*	*0.068*	*0.016*	*0.016*	*0*	*0.01*	*0.01*
SOGI-FLL	*7*	*49.97*	*49.97*	*0.535*	*0.508*	*0.483*	*5.6*	*5.87*	*5.88*
TOGI-FLL	*6.86*	*50.01*	*50.01*	*0.524*	*0.55*	*0.56*	*0*	*0.04*	*0.03*
ESOGI-FLL	*4.85*	*49.98*	*49.98*	*0.000*	*0.029*	*0.028*	*0*	*0.01*	*0.01*
SOGI-FLL	*9.53*	*49.95*	*49.98*	*0.728*	*0.777*	*0.777*	*7.624*	*7.71*	*7.71*
TOGI-FLL	*11.59*	*49.96*	*49.96*	*0.885*	*0.871*	*0.872*	*0*	*0.05*	*0.08*
ESOGI-FLL	*10.05*	*50.01*	*50.01*	*0.000*	*0.045*	*0.043*	*0*	*0.01*	*0.03*
SOGI-FLL	*50*	_	_	_	_	_	_	_	_
TOGI-FLL	*51.7*	*49.38*	*49.48*	*3.950*	*4.13*	*4.181*	*0*	*1.3*	*1.33*
ESOGI-FLL	*47.93*	*49.99*	*49.99*	*0.000*	*0.028*	*0.029*	*0*	*0.08*	*0.09*
SOGI-FLL	*100*	_	_	_	_	_	_	_	_
TOGI-FLL	*100*	_	_	_	_	_	_	_	_
ESOGI-FLL	*99.81*	*50.01*	*50.02*	*0.000*	*0.018*	*0.018*	*0*	*0.03*	*0.03*

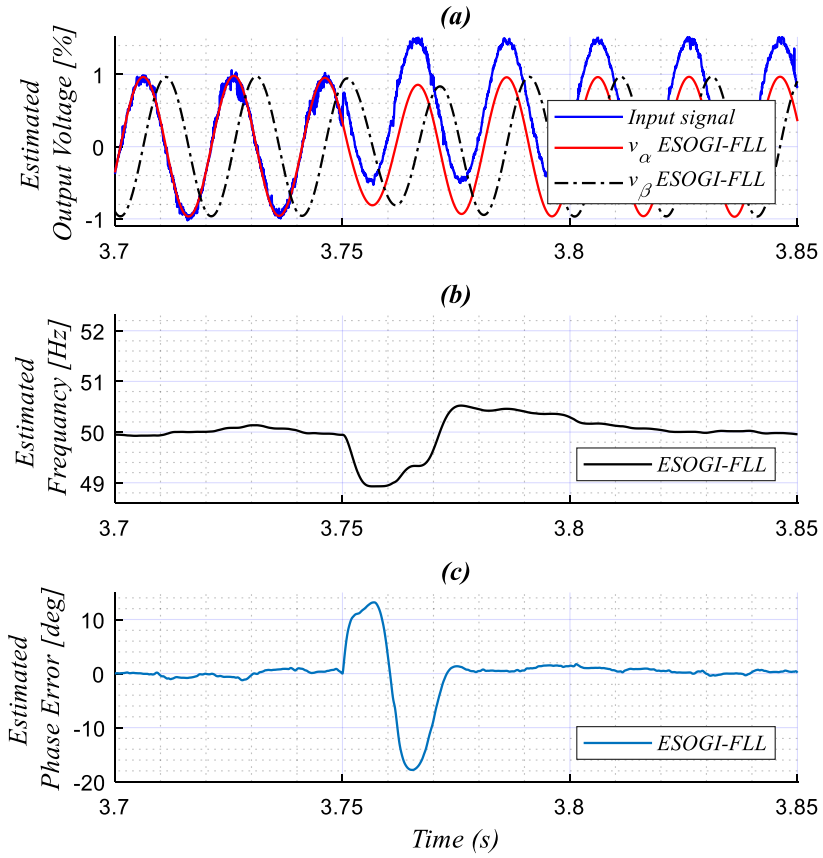


Fig. 2.17. *v_α, v_β, estimated frequency, and phase error for the test of DC-offset variation.*

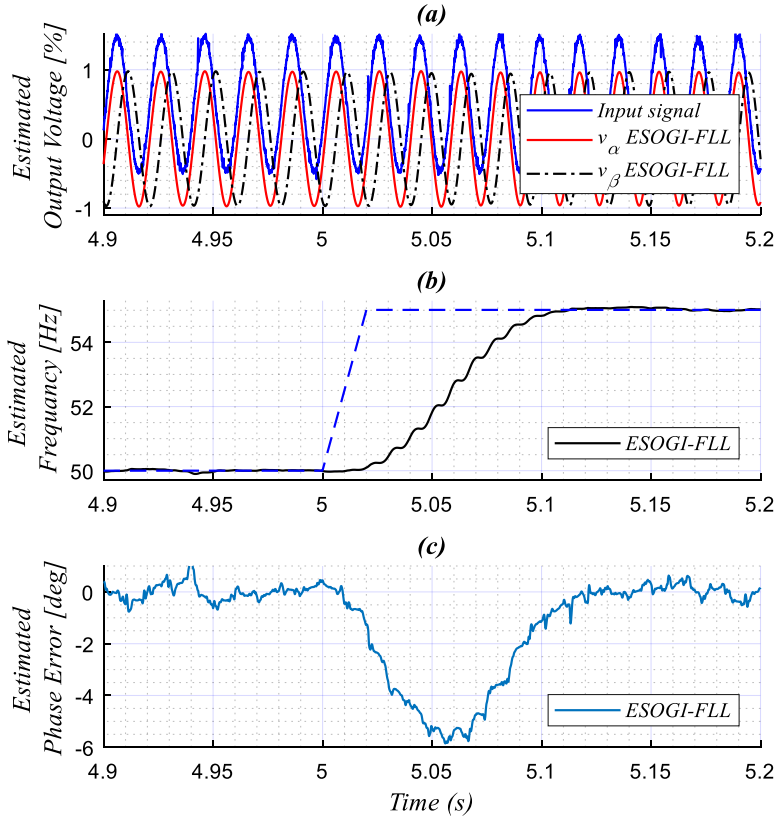


Fig. 2.18. *v_α, v_β, estimated frequency, and phase error for the test of frequency change.*

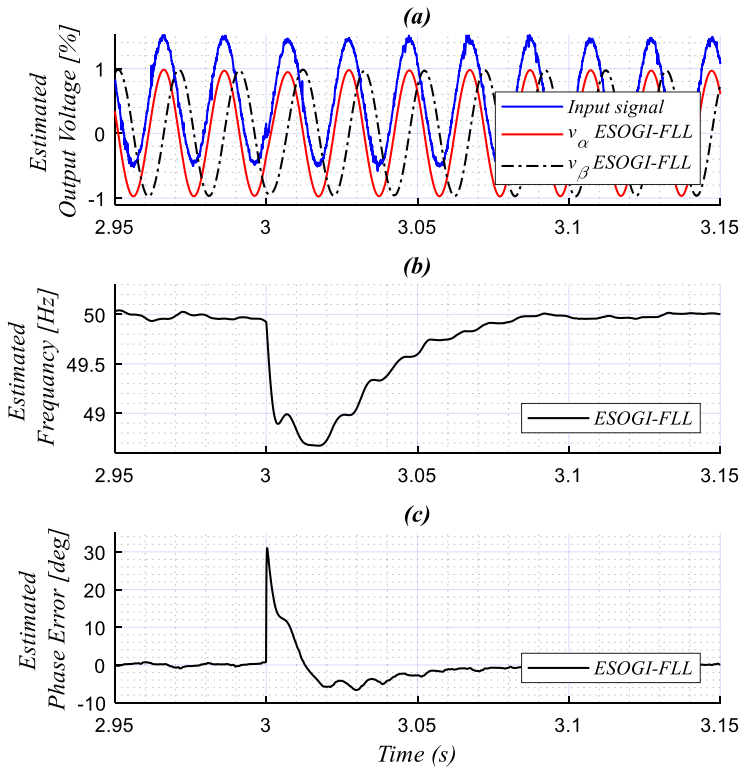


Fig. 2.19. *v_α, v_β, estimated frequency, and phase error for the test of phase jump.*

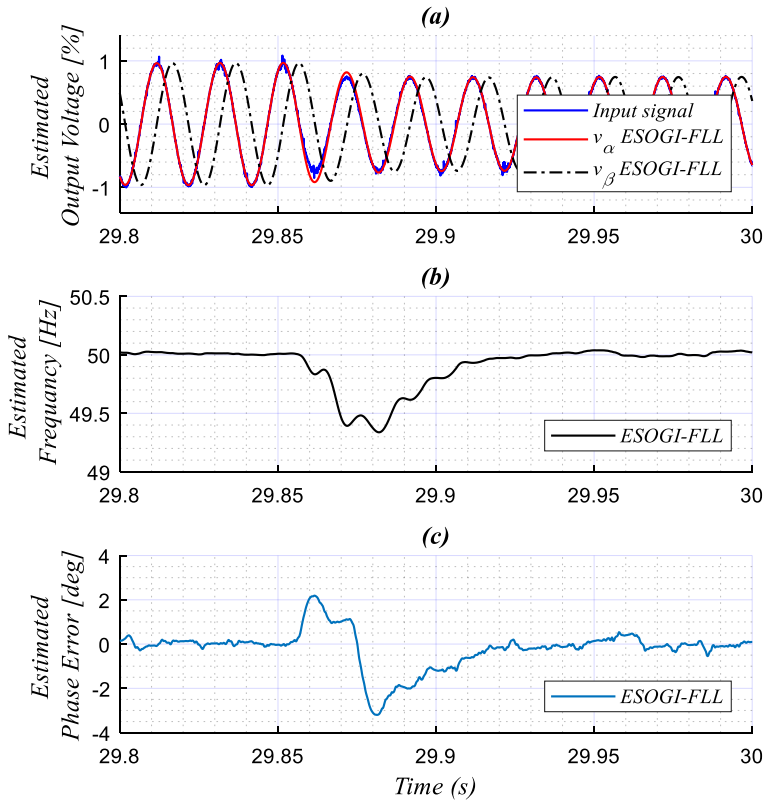


Fig. 2.20. *v_α, v_β, estimated frequency, and phase error for the test of voltage sag.*

2.8 Conclusion

In this chapter, an enhanced scheme for rejecting the effect of the DC component, present in the input voltage, from the estimated parameters has been proposed. The proposed ESOGI-FLL allows the total rejection of DC-offset from the orthogonal component even in case of high DC-offset values. Unlike the traditional SOGI-FLL, the amount of DC-offset in the orthogonal component and ripples amplitude of the estimated frequency and phase have been rigorously determined and eliminated. The simulation study and practical results have demonstrated the good rejection capabilities of the DC component from the estimated parameters when introducing a DC-offset from 10% to 50% in the input signal of its amplitude. In addition, the settling time was found to be 50ms, the same as reported in previous works. The chapter has also reported a detailed comparison of the proposed technique performance with conventional SOGI-FLL and TOGI-FLL to show its effectiveness even when the DC-offset reaches 100%. Regarding the computation burden, the proposed scheme can perform 125 machine cycles, which is relatively low regarding the expected performances. The proposed algorithm was implemented in a low-cost ARM-based microcontroller to confirm the theoretical analysis and the obtained results have been discussed in the present chapter.

Chapter III:

Voltage Tracking Control for Single-phase Inverter in an Islanded Microgrid

Chapter III:

Voltage Tracking Control for Single-phase Inverter in an Islanded Microgrid

The present chapter focuses on designing, modeling, and tuning the inner control including current and voltage control loops for LC-filtered single-phase VSI in autonomous microgrid.

3.1 Introduction

Microgrids include a variety of renewable distributed energy resources (DERs) as a strategy to comply with new environmental standards imposed by state agencies. Typically, DERs need power electronic converters as an interface for connecting to microgrid AC bus, the main grid network and/or local loads [85]. Besides, the converters may have various topologies depending on the application in hand and performance requirements [110]. Voltage source inverters (VSIs) are the most popular option, used to interface distributed generators (DGs) with the microgrid via LC filter, especially during islanded mode when energizing critical loads. Actually, the control of the VSIs is necessary for tracking the inverter output voltage, then, ensure stable and proper operation of the MG. To achieve this objective, an inner control unit is generally involved into the MG primary control for the output voltage tracking. However, this inner controller should provide effective regulations for the dynamics of VSIs in terms of transient and steady-state behavior even under abnormal condition such as: low voltage conditions, voltage unbalances, and frequency perturbations [111].

Numerous control strategies have been developed for designing inner control intended for microgrid systems. Among them, classical linear control system with single or multiple PI feedback/feedforward loops [84], and Proportional-Resonant (PR) control strategies [112—114], and advanced control strategies such as Model Predictive Control (MPC) [115]., and Sliding Mode control (SM) [116]., etc. Paper [117] addresses the implementation of the inner controller based on Proportional-Integral (PI) control methods for single-phase VSI. In [118] a multi-loop resonant controller is proposed for paralleled single-phase droop-controlled inverters in order to improve the output voltage tracking feature. In [119], Finite Control Set-Model Predictive Control (FCS-MPC) strategy has been incorporated in the inner loop to track the voltage reference for an islanded microgrid. This control strategy has provided efficient voltage tracking performance in regard of transient and steady-state responses. Sliding control have been suggested to implement

the inner controller in [120]. The reported performance present tracking of the output voltage with fast speed and high accuracy. Despite the advanced control schemes can provide a superior transient response and a globally stable behavior, they are at times compromised by their complex implementation and parametric sensitivities. However, the control strategies based on PI controller still can ensure output voltage tracking with implementation simplicity, low computational burden, straightforward of modeling and stability analysis, and efficiency under abnormal operating conditions. Besides, the dual-loop inner control scheme is one of the most efficient technique that can guarantee proper regulation of the inverter output voltage. This scheme consists of a voltage control loop (PI), which integrated to adjust the inverter output voltage to the voltage reference provided by the droop stage, and a current PI controller that involved to regulate the inductor current to the current reference generated by the voltage control loop. Further, the techniques using the feed-forward control strategy have found to be effective to track the instantaneous voltage reference by ensuring non-overshoot transient performance. In other hand, the modeling of the inner control loops, stability analysis and the tuning procedure of the controllers' parameters which are essential in order to enable achieving an efficient and robust controller and as a result improve the MG stability.

This chapter introduces the design of an inner control scheme includes a feedforward control strategy for the voltage controller and a proportional (P) controller in the current control loop. In addition, the modeling of the current and voltage control loop for an LC-filtered single-phase VSI as well as the closed-loop model of the inner control are presented. Further, the tuning of the designed controller is performed with the aid of a suggested guideline and analysis based on root locus. By using the obtained closed-loop model, the robustness assessment of the designed controller is verified in front of system parameters variation and voltage reference change. The simulations are carried out with the aid of MATLAB/Simulink/SimPowerSystems environment. The presented results demonstrate the robustness of the proposed controller for the output voltage tracking with good performance in both steady-state and transient conditions and under various abnormalities. The validity of the designed controller is confirmed through experimental tests based on ARM cortex microcontroller.

3.2 Proposed inner control for droop-controlled MG

The schematic diagram of the double-loop inner control-based primary control for single-phase droop-controlled VSI is presented in **Fig. 3.1**. The power stage consists of a DG DC source, voltage source inverter (VSI) and an LC filter associated to an AC bus, where the load is connected, via a line impedance. The inner control scheme comprises of a voltage controller of

instantaneous output voltage and the current controller of instantaneous filter-inductor current. The voltage controller is in charge of tracking the voltage reference, while the current controller is used to speed up the system response. As shown in this figure, the control loops require the droop voltage reference and measurements, which are the output and the inductor currents, and the voltage of the inverter and of the capacitor. In **Fig. 3.2**, more detailed scheme of the proposed voltage and current control loops is depicted. As shown, the voltage controller introduces an IP-type regulator in order to regulate the voltage capacitor to the desired voltage reference provided by the droop control stage. This type of regulator can guaranty good transient response with non-overshoot. The current control loop integrates a PI regulator in order to adjust the inductor current to the current reference generated by the voltage controller and to produce modulating signals for the inverter switches through a PWM module. It is worth noting that the current control loop is the fastest loop in the proposed multi-loop control scheme, in which its time response should set at least one order faster than the voltage regulator [121].

The design of the output voltage control scheme should ensure every VSI module perform as a robust voltage source, in order to reduce the impact of VSIs' internal impedance on the system control performance. To this regard, the modeling, analysis and tuning procedure of the inner voltage and current controller for a single-phase VSI are presented in the following section.

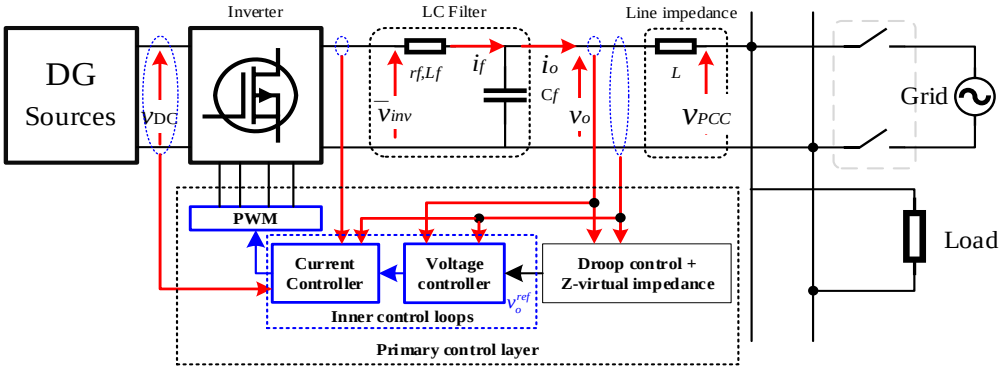


Fig. 3.1. *schematic of the inner controller-based primary control for a single-phase VSI.*

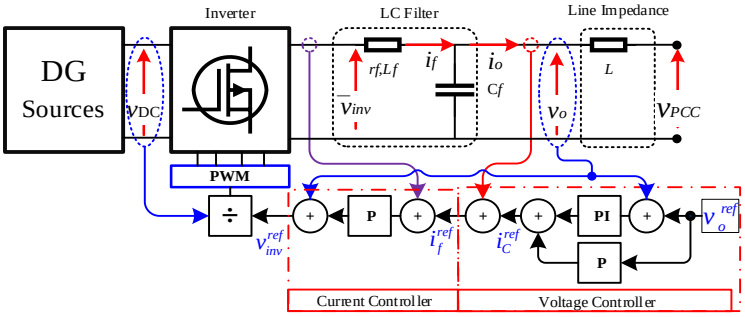


Fig. 3.2. *Block diagram of the multi-loop controller including IP-type voltage controller and a P current controller.*

3.3 Modeling and analysis of the inner control loops for single-phase VSI

In this section, the modeling of the inverter with an LC filter is presented and the proposed control strategy is developed. In addition, the closed-loop model of the system incorporating the considered control strategy is derived. Further, a guideline for the tuning of the controller parameters is also adopted in this section.

3.3.1 Modeling of the LC-filtered VSI

According to **Fig. 3.2**, the mathematical formulation of the single-phase inverter VSI with LC filter can be given as follow:

$$L_f \frac{d}{dt} i_f(t) = \bar{v}_{inv}(t) - r_f i_f(t) - v_o(t) \quad (3.1)$$

$$C_f \frac{d}{dt} v_o(t) = i_f(t) - i_o(t) \quad 3.2)$$

$$\bar{v}_{inv}(t) = D v_{DC}(t) \quad 3.3)$$

where $\bar{v}_{inv}$ is the average value of the output voltage of the inverter side, v_o, i_o and i_f are the output voltage and current of the LC-filtered inverter side, and the inductor filter current, respectively. L_f, r_f, and C_f define the inductance and resistance of the filter indictor, and the filter capacitor, respectively. D represents switching action depending on the state of the pair of switches Q_1-Q_3 and Q_2–Q_4, which can take the values belong to the interval [-1, 1].

The transfer functions of **Eqs**. **(3.1)** to **3.3)** can be rewritten in the *s*-domain as:

$$G_f(s) = \frac{i_f(s)}{\bar{v}_{inv}(s) - v_o(s)} = \frac{1}{L_f s + r_f} \quad 3.4)$$

$$G_o(s) = \frac{v_o(s)}{i_f(s) - i_o(s)} = \frac{1}{C_f s} \quad 3.5)$$

$$\bar{v}_{inv}(s) = D v_{DC}(s) \quad 3.6)$$

Accordingly, the schematic diagram of the averaged model of an inverter with LC filter in *s*-domain can be obtained as shown in **Fig. 3.3**. The system model, as shown, includes the model of the filter inductor and capacitor. It is worth to note that the big symbols define the average values of the corresponding variable.

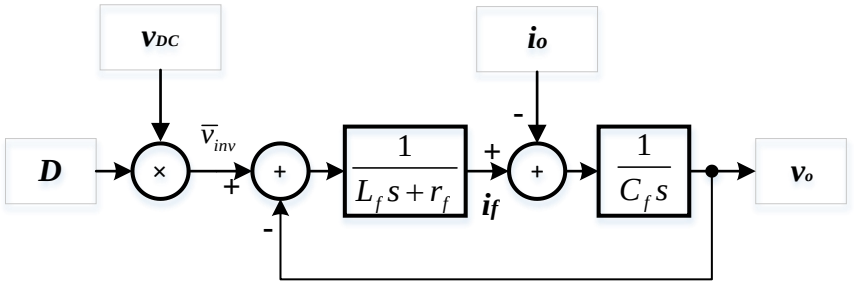


Fig. 3.3. Block diagram of the LC-filtered inverter model.

3.3.2 Control strategy

As afore-mentioned, an IP-type controller is introduced for the voltage regulator while a proportional P controller is used in the current control loop.

In the current controller loop, the measured current i_f is compared to the corresponding i_f^{ref} reference, as shown in Fig. 3.3. The obtained current error is presented to a proportional controller k_{P-If} to generate the average value of the output voltage reference of the inverter side, v_{inv}^{ref}, in corporation with the output voltage v_o. Then, the expression of the current compensator can be written as follows:

$$v_{inv}^{ref} = k_{P-If}\left(i_f^{ref} - i_f\right) + v_o \tag{3.7}$$

where the second term + v_o is the compensation term.

In the voltage control loop, proportional-integral (PI) control with proportional (P) feedforward compensation is proposed. An error is measured between the actual output voltage v_o of the LC-filter side and its reference v_o^{ref}. This error and the voltage reference v_o are handled by the designed controller. The output current i_o of the inductor is added to the output of controller for producing the current reference i_f^{ref} of the inductor. Accordingly, the voltage compensator can be expressed as follows:

$$i_f^{ref} = \left(k_{P-E} + \frac{k_{I-E}}{s}\right)\left(v_o^{ref} - v_o\right) - k_{P-E}v_o^{ref} + i_o \tag{3.8}$$

where k_{P-E} and k_{I-E} are the control gains.

By the way, the parameters k_{P-I}, k_{P-E}, and k_{I-E} of the current and voltage compensators should be properly tuned to provide an effective transient response and good performance at steady state. To this end, a tuning procedure for the selection of the controllers' gains is presented

in the following section.

3.3.3 Parameters' control tuning

Tuning a controller is an important task in the control system because a good controller tuning can ensure high efficiency, low energy cost, increased production rate and reduced process variability. This section presents a guideline for the tune that adapts the PI parameters in order to steer the closed-loop response to satisfy preset time-domain desired specifications.

Besides, to attain proper selection the parameters of the current controller and the voltage controller, the closed-loop models of LC-filtered VSC incorporating the designed controllers should be derived.

Fig. 3.4 illustrates the block diagram of the inner control closed-loop model. According to this figure, the closed loops model consists of the system model, i.e., VSI with LC filter, the functions of the controllers, and the transfer function ***T(s)*** describing the time delay dynamics, which can be expressed by its one of the simplest linear approximations as follows:

$$T(s) = \frac{D(s)}{D^{ref}(s)} = \frac{1 - \frac{T_s s}{2}}{1 + \frac{T_s s}{2}} \tag{3.9}$$

Being T_s the sampling time, and D^{ref} the duty ratios of the PWM, given in **Fig. 3.4**, that can be defined as a function of the average value of the output voltage reference of the inverter side and the DC side voltage as follows:

$$D^{ref} = \frac{\overline{v}_{inv}^{ref}}{v_{DC}} \tag{3.10}$$

Fig. 3.5 (a) and **Fig. 3.6 (a)** depict the block diagram of the closed-loop models of the current and voltage for a LC-filtered VSI. From these figures the mathematical formulation of the closed-loop models can be obtained as follows:

$$i_f = G_{If-if} i_f^{ref} - G_{If-vo} v_o \tag{3.11}$$

$$v_o = G_{vo-vo} v_o^{ref} - G_{vo-io} i_o \tag{3.12}$$

where the transfer functions G_{If-if}, G_{If-vo}, G_{vo-vo}, and G_{vo-io} are given below:

$$\begin{cases} G_{If-if} = \dfrac{i_f}{i_f^{ref}} = \dfrac{k_{P-If}\left(1-\dfrac{T_s s}{2}\right)}{\left[\dfrac{L_f T_s}{2}\right]s^2+\left[L_f+\left(r_f-k_{P-If}\right)\dfrac{T_s}{2}\right]s+\left[r_f+k_{P-If}\right]} \\ G_{If-vo} = \dfrac{i_f}{v_o} = \dfrac{T_s s}{\left[\dfrac{L_f T_s}{2}\right]s^2+\left[L_f+\left(r_f-k_{P-If}\right)\dfrac{T_s}{2}\right]s+\left[r_f+k_{P-If}\right]} \end{cases} \quad \textbf{3.13)}$$

$$\begin{cases} G_{vo-vo} = \dfrac{b_{11}s+b_{10}}{a_4 s^4+a_3 s^3+a_2 s^2+a_1 s+a_0} \\ G_{vo-io} = \dfrac{s\left(b_{22}s^2+b_{21}s+b_{20}\right)}{a_4 s^4+a_3 s^3+a_2 s^2+a_1 s+a_0} \end{cases} \quad \textbf{3.14)}$$

with the following parameters:

$$\begin{cases} a_0 = k_{P-If}\,k_{I-E} \\ a_1 = k_{P-If}\left[k_{P-E}-\dfrac{T_s}{2}k_{I-E}\right] \\ a_2 = \left[T_s-\dfrac{T_s}{2}k_{P-If}\,k_{P-E}+C_f\left[r_f+k_{P-If}\right]\right] \\ a_3 = C_f\left[L_f+\left(r_f-k_{P-If}\right)\dfrac{T_s}{2}\right] \\ a_4 = \left[\dfrac{C_f L_f T_s}{2}\right] \end{cases}, \text{ and } \begin{cases} b_{10} = k_{P-If}\,k_{I-E} \\ b_{11} = -\dfrac{T_s}{2}k_{P-If}\,k_{I-E} \\ b_{20} = r_f \\ b_{21} = L_f+\dfrac{T_s}{2}r_f \\ b_{22} = \dfrac{L_f T_s}{2} \end{cases}$$

By assuming that the time delay is negligible, hence, the transfer function of **Eq. 3.13)** result in:

$$\begin{cases} G_{\substack{If-if \\ simplify}} = \dfrac{i_f}{i_f^{ref}} = \dfrac{k_{P-If}}{L_f s+\left(r_f+k_{P-If}\right)} \\ G_{\substack{If-vo \\ simplify}} = \dfrac{i_f}{v_o} = 0 \end{cases} \quad \textbf{(3.15)}$$

In addition, based on the hypothesis that the current controller is faster compared to the voltage controller, thus, the current control loop is considered in steady-state and its closed-loop transfer function can be given as follow:

$$\begin{cases} G_{\substack{If-if \\ simplify}}(s)\Big|_{Steady-stat} = \left|G_{\substack{If-if \\ simplify}}\right| \to 1 \\ G_{\substack{If-vo \\ simplify}}(s)\Big|_{Steady-stat} = \left|G_{\substack{If-vo \\ simplify}}\right| = 0 \end{cases} \quad (3.16)$$

Further, according to **Eq. (3.13),** the closed-loop transfer function of the voltage control loop, can be derived as follows:

$$\begin{cases} G_{\substack{vo-vo \\ simplify}}(s) = \dfrac{\dfrac{k_{I-E}}{C_f}}{s^2 + \dfrac{k_{P-E}}{C_f}s + \dfrac{k_{I-E}}{C_f}} \\ G_{\substack{vo-if \\ simplify}}(s) = 0 \end{cases} \quad (3.17)$$

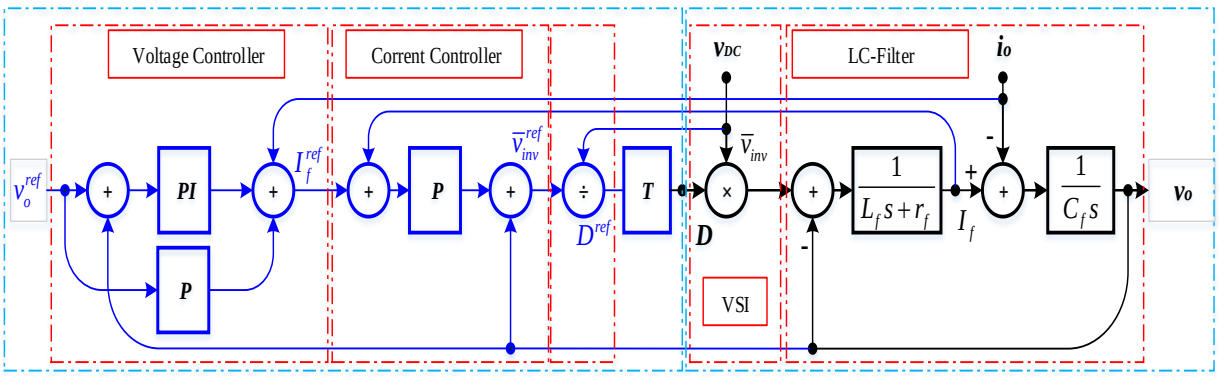


Fig. 3.4. *Closed-loop model of voltage-controlled LC-filtered VSC.*

The transfer functions $\boldsymbol{G_{If-if}}$ and $\boldsymbol{G_{vo-vo}}$, which represent the closed-loop model of the current and voltage control loops, are first-order and the second-order transfer functions (see **Fig. 3.5 (b)** and **Fig. 3.6 (b)),** respectively.

Thus, by matching these obtained models with desired fist order and second-order transfer functions, given below:

$$G_{\substack{If-if \\ simplify}}(s) = k_{If}\frac{1}{\tau s + 1} \quad (3.18)$$

$$G_{\substack{vo-vo \\ simplify}}(s) = k_v \frac{\omega_v^2}{s^2 + 2\zeta_v\omega_v s + \omega_v^2} \quad (3.19)$$

The expressions of the parameters $\boldsymbol{k_{If}}$, $\boldsymbol{\tau}$, $\boldsymbol{k_v}$, $\boldsymbol{\xi_v}$ and $\boldsymbol{\omega_v}$ can be derived as follows:

$$\begin{cases} k_{If} = \dfrac{k_{P-If}}{k_{P-If} + r_f} \cong 1 \\ \tau = \dfrac{L_f}{k_{P-If} + r_f} \end{cases}, \text{ and } \begin{cases} k_v = 1 \\ \zeta_v = \dfrac{k_{P-E}}{2}\sqrt{\dfrac{1}{C_f k_{I-E}}} \\ \omega_v = \sqrt{\dfrac{k_{I-E}}{C_f}} \end{cases} \tag{3.20}$$

where k_{If} and τ stand for the gain factor and the time constant of the inner control loop and k_v, ξ_v and ω_v stand for the gain factor, the damping factor and the natural frequency of the outer control loop respectively.

Based on **Eq. (3.20)**, the parameters of current and voltage controllers can be expressed as follow:

$$\begin{cases} k_{P-If} = \dfrac{L_f - r_f \tau}{\tau} \\ \begin{cases} k_{P-E} = 2C_f \zeta_v \omega_v \\ k_{I-E} = C_f \omega_v^2 \end{cases} \end{cases} \tag{3.21}$$

According to the equation above, a precise selection of the controllers' coefficients that can offer optimal transient responses, can be achieved by choosing the parameters τ, ξ_v and ω_v. These parameters, in turn, can be determined from the transient response overshoot M_P and the settling time T_s, based on the following equations:

$$\begin{cases} T_{S-If} = 4\tau \\ M_{P-E} = e^{\frac{\zeta_v \pi}{\sqrt{1-\zeta_v^2}}} \\ T_{S-E} = \dfrac{4}{\zeta_v \omega_v} \end{cases} \tag{3.22}$$

It is worth mentioning those the values of the damping factor and settling time are chosen according to the analysis based on root-locus plots, while considering the following conditions:

$$\begin{cases} f_n \; \dfrac{1}{T_{S-E}} \; \dfrac{4}{T_{S-If}} \; f_{rs} \; \dfrac{f_{switch}}{2} \\ 0.4 \le \zeta_v \le 1 \end{cases} \tag{3.23}$$

By adjusting one of the parameters each time, the impact of each parameter on system performance is analyzed. The parameters range, which ensures the system stability, can be

obtained. According to the pole distribution, the current and voltage control parameters, which help achieve a desired performance for the system, can be acquired.

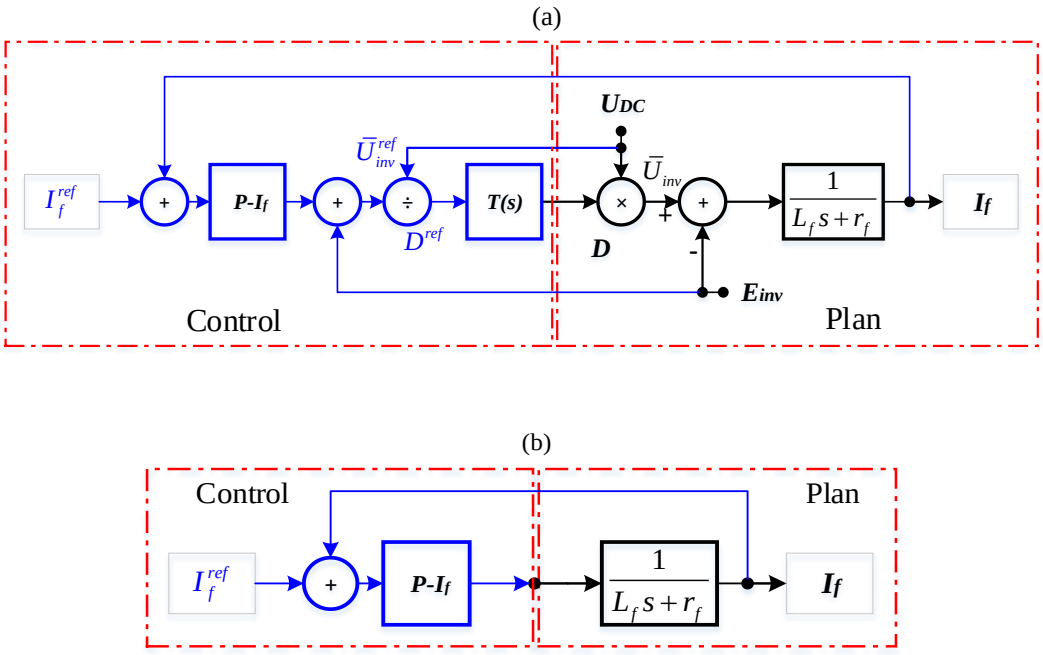


*Fig. 3.5. The closed-loop model of the current control loop, **(a)** complete model and **(b)** simplified model.*

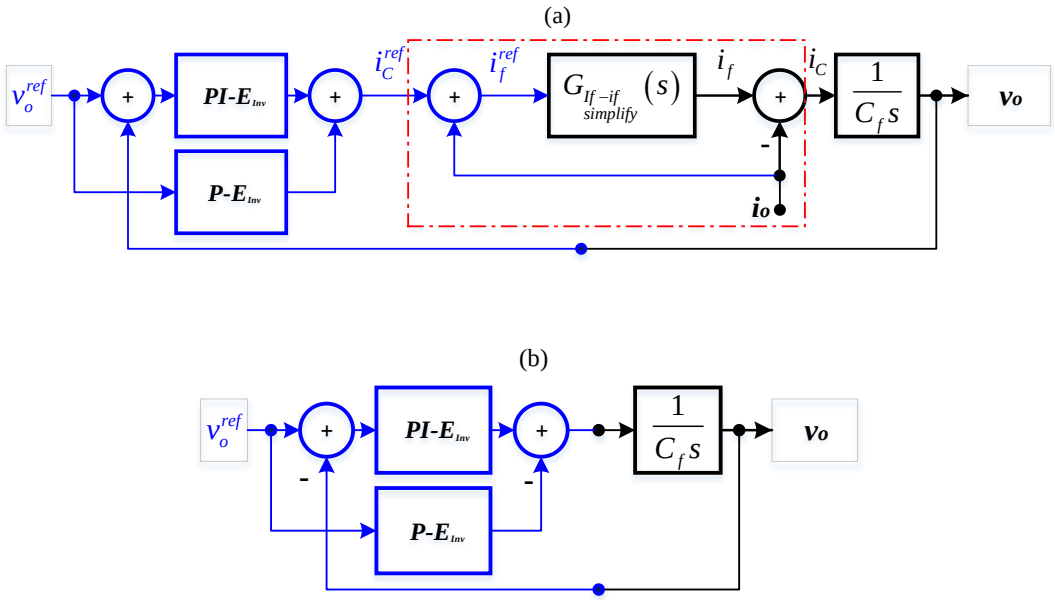


*Fig. 3.6. The closed-loop model of the voltage control loop, **(a)** complete model and **(b)** simplified model.*

3.3.4 Sensitivity assessment to the control parameters

The influence of the settling time T_{s-if} is shown in **Fig. 3.7**, in which the curve representing the root-locus corresponding to the change of T_{s-if} is pointed out. As illustrated in the figure, there is one couple of roots in the current control loop. In addition, with proportionality in increasing the settling time T_{s-if}, a couple of the root moves to convergence until they are equal in value on the real axis of the positive part, they then correspond to the real axis with complex values, In this part, a couple of the root decrease in the real part and the imaginary part diverges and then converges until they are gone, thereupon a couples of the root is equal in value on the real axis of the negative portion, then they diverge with keeping negative real values.

In fact, the optimal controller parameters can be chosen when a couple of the root is near from real-axis of the negative part, therefore, the value of the settling time $T_{s\text{-}If}$ can be chosen as:

$$T_{S-If} \geq 5.31\times10^{-4}\ s \tag{3.24}$$

The influence of the settling time T_{s-vo} , T_{s-if} and the damping factor ξ_v in moves of the roots of the voltage control loop are illustrated in **Fig. 3.8 (a)**. Note that curves representing the root-locus are obtained by fixing both T_{s-if} and ξ_v at the specified values and increasing T_{s-vo} for each curve.

As seen, when increasing the damping coefficient value ξ_v, meanwhile, the settling time T_{s-if} is chosen in the section that achieves the current control loop stability, the roots move to the stable region. One can be noticed that the damping coefficient ξ_v can be determined to achieves the possibility of a curve in part of all roots near from the real axis in the negative part. Then, the value of the damping coefficient can be determined as follows:

$$0.6 \leq \zeta_v \tag{3.25}$$

As shown in **Fig. 3.8 (b)**, which clarifies the possibility to determine the settling time T_{s-vf}, which achieves the voltage control loop stability. One can be concluded that this parameter can selected as follows:

$$T_{S-vo} \geq 3.078\times10^{-3}\ s \tag{3.26}$$

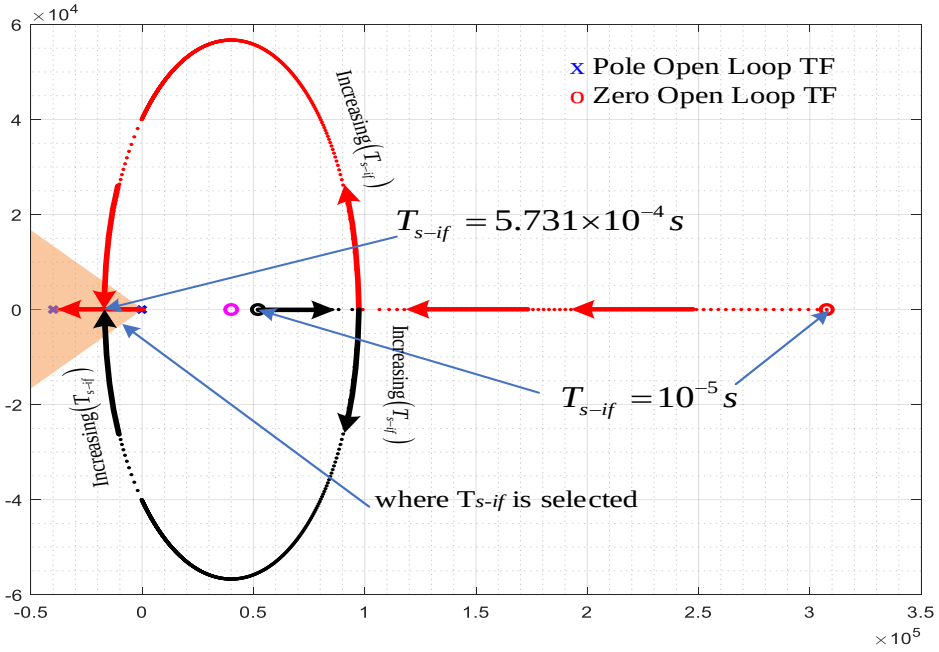


Fig. 3.7. *Root-locus corresponding to the change of parameter* $\boldsymbol{T_{s-if}}$.

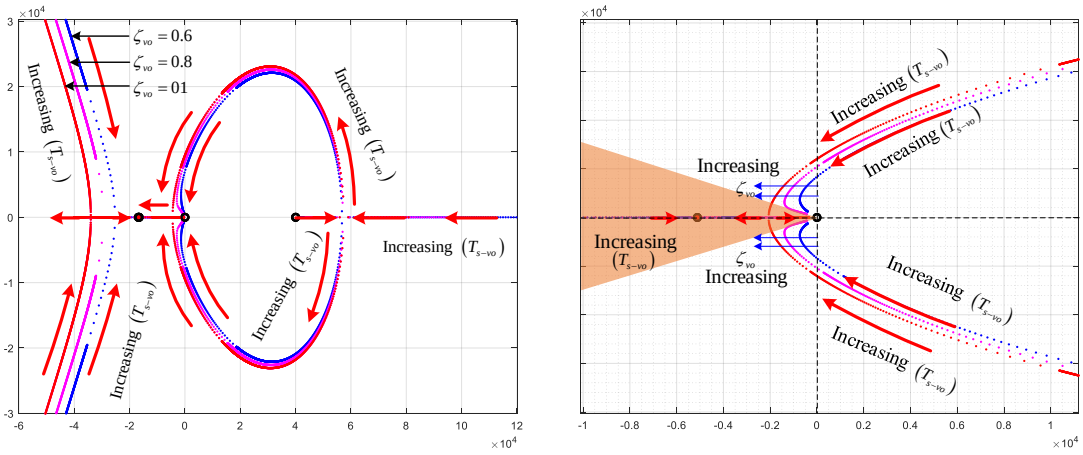


Fig. 3.8. *Root-locus corresponding to the change of the parameter* $\boldsymbol{T_{s-vo}}$.

3.4 Robustness assessment of the designed controllers

In order to evaluate the robustness of the designed current and voltage controllers for current and voltage references change and system parameters variation, a simulation study in MATLAB/ Simulink is carried out. In this study, the transient performances of the obtained inner control closed-loop model, given in **Fig. 3.4**, in response to change in the voltage and the current references are evaluated. In addition, the influence of the system parameters $\boldsymbol{L_f, r_f, C_f,}$ and $\boldsymbol{T_s}$ variation in the roots of the closed-loop model is investigated.

The obtained simulation results in response to the references change of the current and voltage are depicted in **Fig. 3.9 (a), (b)** and **(c)**, and scopes the transient performances of the capacitor voltage, and inductor current and their corresponding references, and the output current, respectively. According to these figures, one can notice that the designed controllers can track perfectly the desired references, and are not influenced by the linear and no-linear load changes.

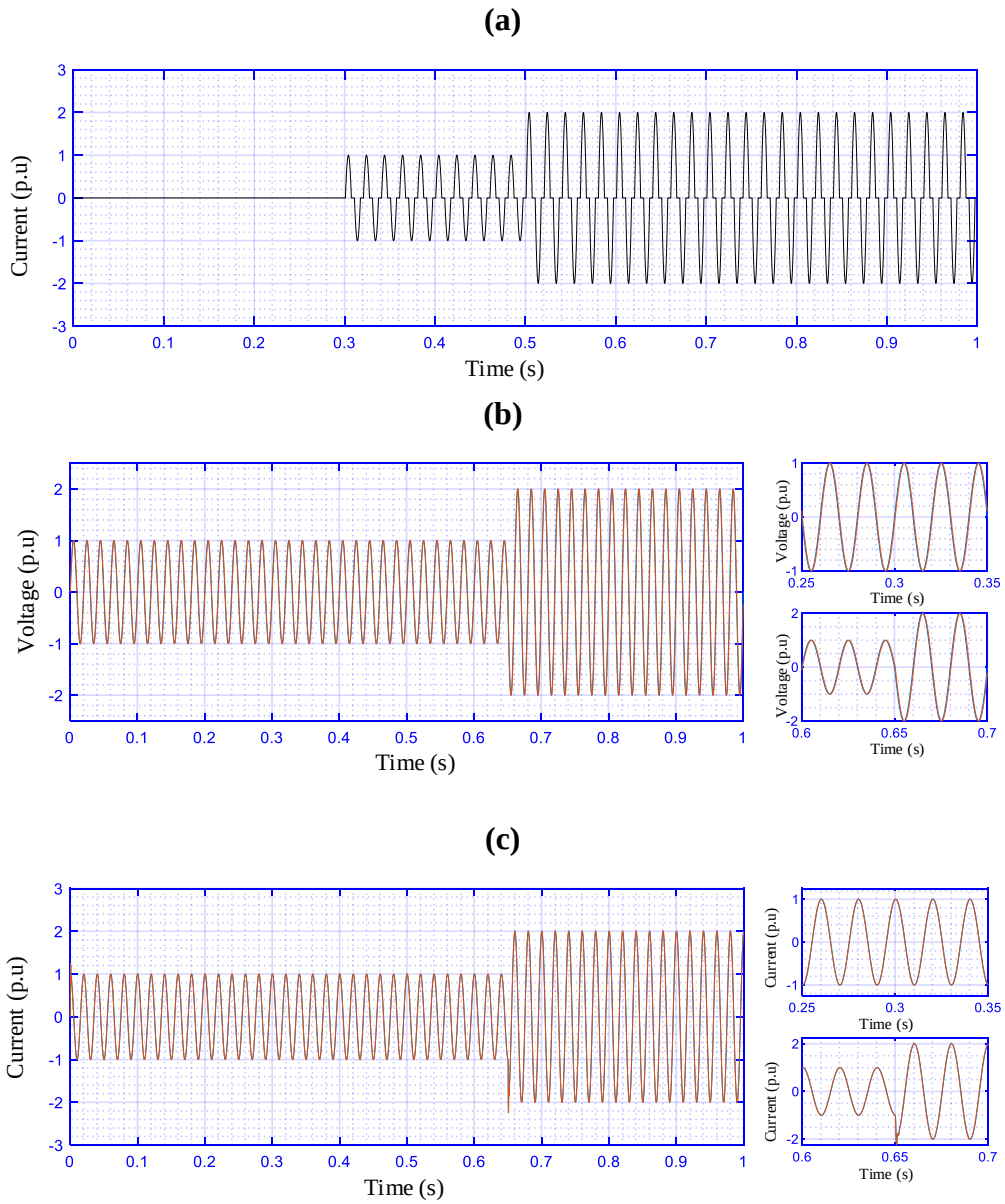


Fig. 3.9. *Inner control performance in response to voltage reference step change,* ***(a)*** *output current,* ***(b)*** *output voltage, and* ***(c)*** *inductor current.*

The performance of the control system is investigated in terms of stability, considering variations in L_f, r_f, C_f, **and** T_s values, and the results are shown in **Fig. 3.10 (a)** to **(c)**. Through this study, the range of the system parameters changes can be determined, where the voltage control system remains stable. Obviously, the proposed design values of current and voltage

controllers give high dynamic performance and robust stability under parameters variation.

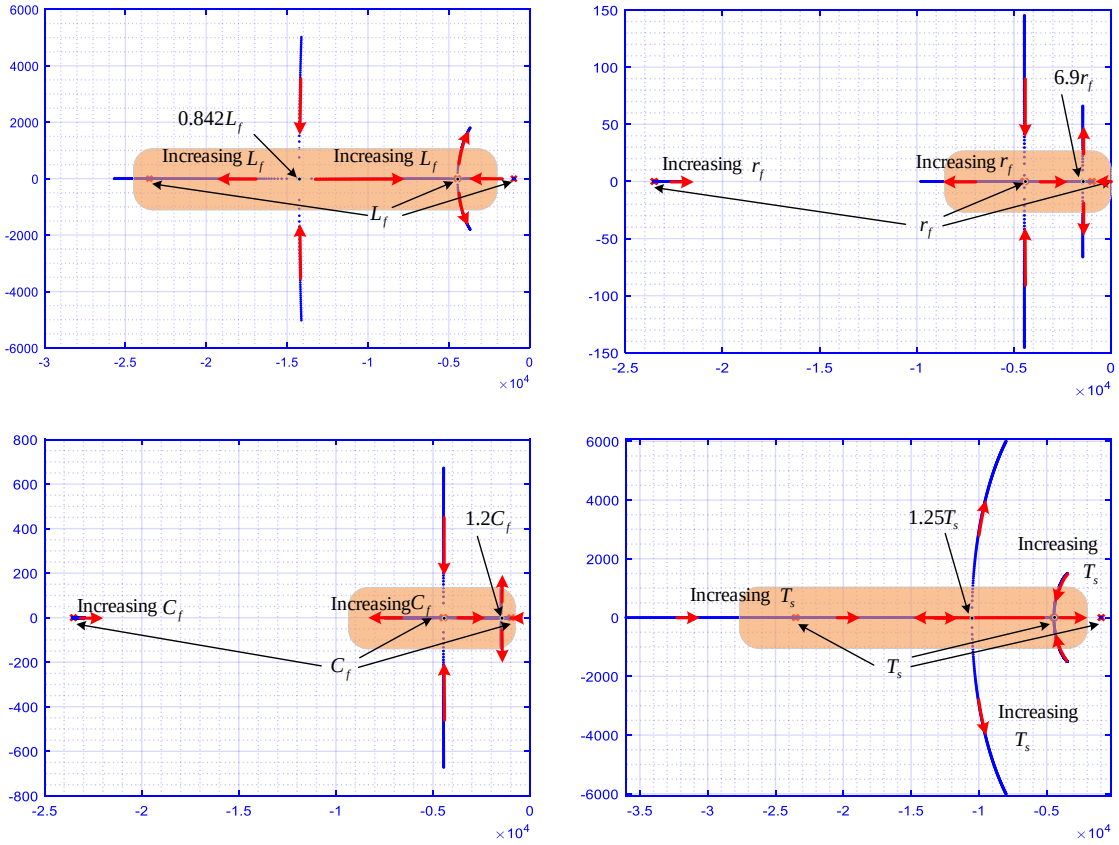


Fig. 3.10. Root-locus corresponding to the change of parameter T_{s-vo}.

3.5 Discrete time implementation of the inner controller:

It is well known that a controller should discretize, at first, in order to be implemented in microcontroller. Therefore, the discrete implementation of the current and voltage controllers is described below. In fact, the trapezoidal method is used to implement a discrete-time integrator, which can be presented by the following formulation;

$$y(k) = y(k-1) + \frac{T_s}{2}\left[u(k) + u(k-1)\right] \tag{3.27}$$

where *y (k)* and *y(k-1)* the actual and previous values of the output voltage, while *u(k)* and *u(k-1)* are the actual and previous input voltages of the integrator. *k* defines operator of the discrete time domain.

It is worth noting that in this method, the integral operator in *s*-domain, i.e., $\frac{1}{s}$, is approximated by [109]:

$$\frac{1}{s} = \frac{T_s}{2}\frac{1+z^{-1}}{1-z^{-1}} \tag{3.28}$$

where ***z*** denotes the discrete *z*-domain operator.

By replacing **Eq. (3.27)** in **Eqs. (3.1)** to **(3.3)**, the expression of the inner controller in discrete time can be obtained as follows:

$$i_f^{ref}(z) = \left(k_{P-E} + k_{I-E}\frac{T_s}{2}\frac{1+z^{-1}}{1-z^{-1}}\right)\left(v_o^{ref}(z) - v_o(z)\right) - k_{P-E}v_o^{ref}(z) + i_o(z) \tag{3.29}$$

Accordingly, the model of inner controller in discrete time can be presented by:

$$\begin{cases} x(k) = x(k-1) + \left[v_o^{ref}(k) - v_o(k)\right] \\ i_f^{ref}(k) = i_o(k) - k_{P-E}v_o(k) + k_{I-E}\dfrac{T_s}{2}\left[x(k) + x(k-1)\right] \\ \bar{v}_o^{ref}(k) = k_{P-If}\left[i_f^{ref}(k) - i_f(k)\right] + v_o(k) \\ D^{ref}(k) = \dfrac{\bar{v}_o^{ref}(k)}{v_{DC}(k)} \end{cases} \tag{3.30}$$

where ***x(k)*** is the state variable.

3.6 Simulation results

The aim of this section is to evaluate the performance of the designed inner control loops for single-phase VSIs under different operating conditions. The considered performance criteria are the transient and steady state responses behavior and the waveforms of the inverter current and voltage. A system shown in **Fig. 3.11**, which consist of DC source feeds a VSI with an LC filter, which in turn supply a local load, is built up in MATLAB/Sim power system. The inverter is controlled by the designed multi-loop inner control, including the voltage controller responsible of tracking the output voltage reference imposed by the droop control unit and the current controller in charge of regulating the inductor current to the current reference produced by the voltage control loop and generating the modulation signals which derive the bridge converter. The parameters of the simulated system are given in **Table 3.1**.

The designed controller is tests considering the case studies listed below:

- Case study 01: a change of the amplitude of the output voltage reference from 220V to 176V of fundamental amplitude is performed at **t = 01s**.
- Case study 2: a step change of the inverter frequency is happened at **t = 0.5s**.

- Case study 3: a phase jump is introduced into the output voltage reference at **t = 1.5s**.

The obtained simulation results of the performance tracking of the controller regarding the instantaneous output voltage and current, and phase angle in response to case studies, 1, 2 and 3, are demonstrated in **Fig. 3.11**,**Fig. 3.12,** and **Fig. 3.13**, respectively.

Table 3.1. *Parameters of the simulation study*

Parameters	Symbol	Unit	Value
Nominal Voltage	E_n	V	220
Nominal frequency	f_n	Hz	50
Switching frequency	f_s	kHz	20
Simulation frequency	f_s	MHz	1
DC voltage	U_{DC}	V	495
Output filter capacitor	C	µF	23
Output filter inductor	L,r	mH, Ω	2, 1
Line impedance of DG	L	mH, Ω	0.5,0.8
Voltage controller P gain	k_{pv}	-	0.1839
Voltage controller I gain	k_{pi}	-	183.87
Current controller P gain	k_{iv}	-	6.2831

Fig. 3.11 proves the effective operation from the current control loop, in which the inductor current follows the reference current established by the voltage control loop and when changing the amplitude value of the voltage reference (curve (b)). The same performance for the output voltage and its reference are remarked (curve (a)). These figures show proper transient response with fast speed, a settling time around t_s **= 20 ms**, and without overshot. **Fig. 3.12** demonstrates that the output current and voltage of the inverter tacks the current and voltage references, even when the operating frequency changes. It is ensuing, as well, faster and accurate transient response, t_s = 20 ms, without overshoots and zero error in steady state. The result presented by **Fig. 3.13** shows the stable operation of the system against phase jump, in which effective tracking performance of the current and voltage are achieved.

From the given figures, one can be remarked that the phase of the input matches with the output voltage phase.

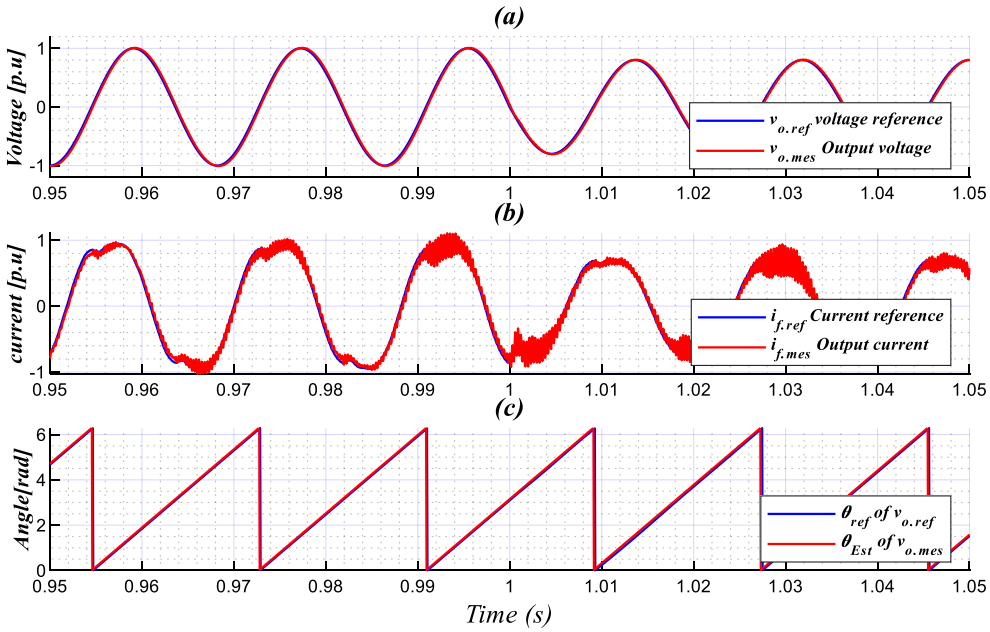


Fig. 3.11. *Simulation results in response to case 1.*

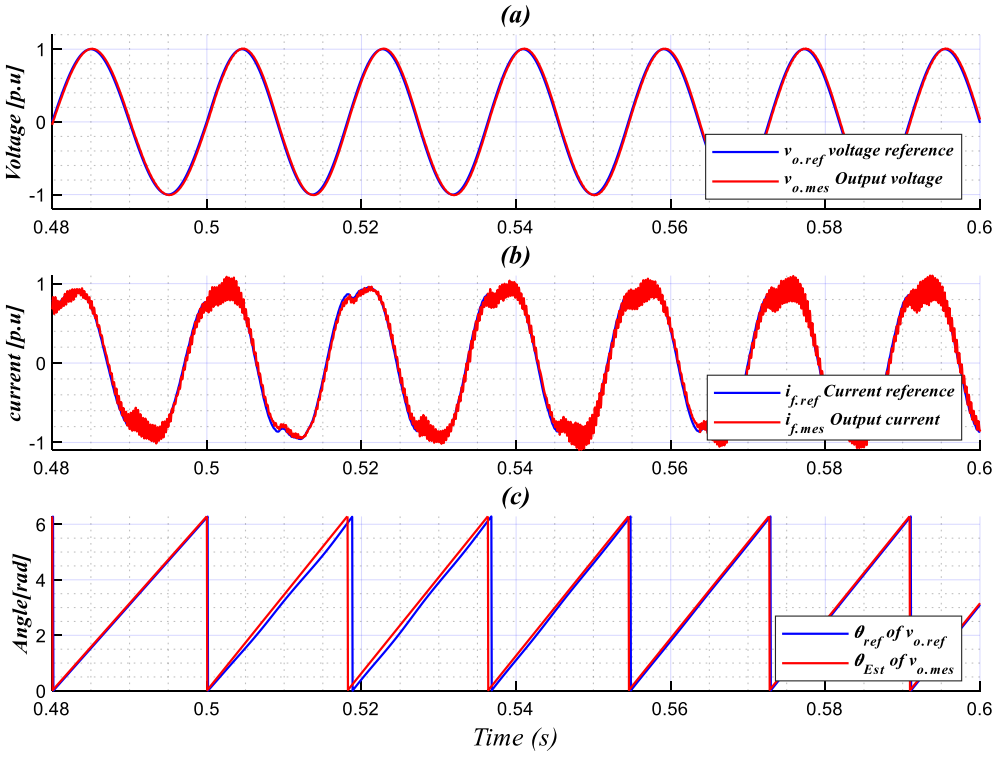


Fig. 3.12. *Simulation results in response to case 2.*

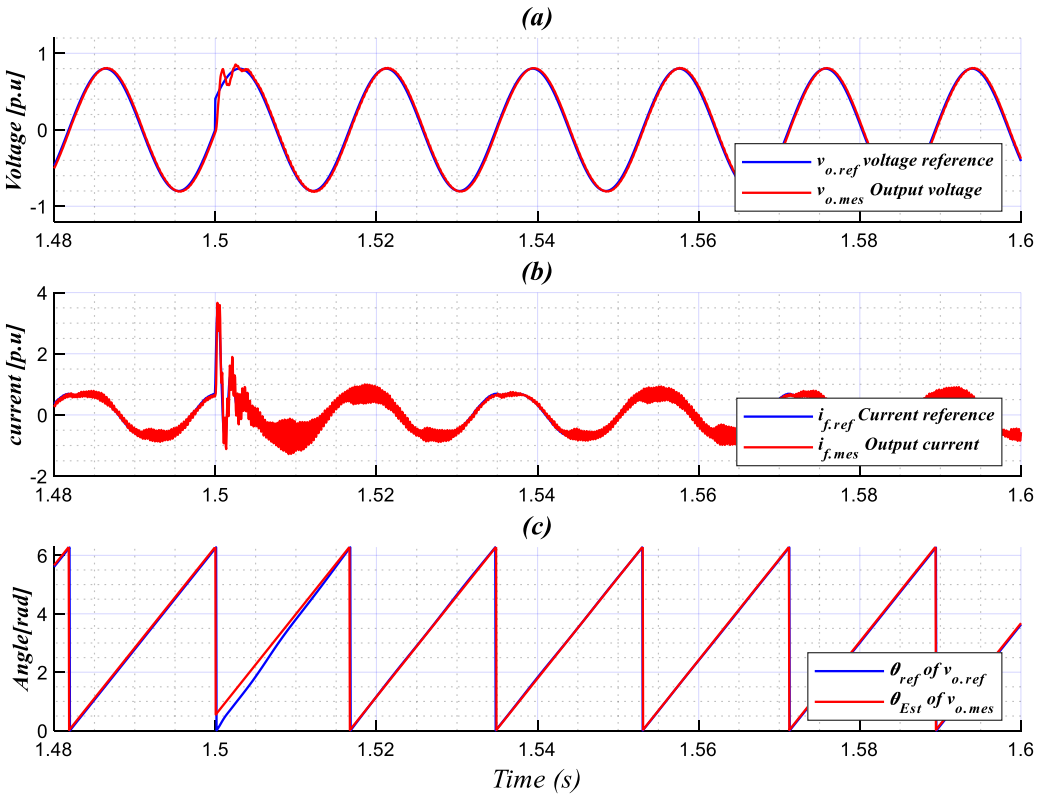


Fig. 3.13. *Simulation results in response to case 3.*

3.7 Experimental implementation

The focus of this section is to implement the proposed current and voltage loops for the control of a single-phase VSI. A system is built in which the inner control algorithm is implemented in an ARM Cortex Microcontroller. The same tests are considered as the ones presented in the simulation study.

Fig. 3.14, Fig. 3.15 and **Fig. 3.16** show the performance of the proposed controller for the performed tests. The voltage performance from the voltage control loop shown in **Fig. 3.14 (a)** illustrates precise tracking of the voltage reference when the voltage amplitude change (*at t=*, in which it reaches the reference with a setting time t_s = 0.02 s. **Fig. 3.14 (f)** demonstrates that the actual voltage angle phase track perfectly the angle phase of the voltage reference.

From **Fig. 3.15**, one can be seen that the accurate tracking of the output voltage and angle phase is achieved when the frequency change. In addition, a pure sinusoidal output voltage is obtained. **Fig. 3.16** validates the effective tracking of the output voltage reference after an angle phase jump occurs. Also, it demonstrates a stable single-phase sinusoidal waveform of the output voltage. The obtained result reveals the stable operation of the single-phase VSI under different disturbances.

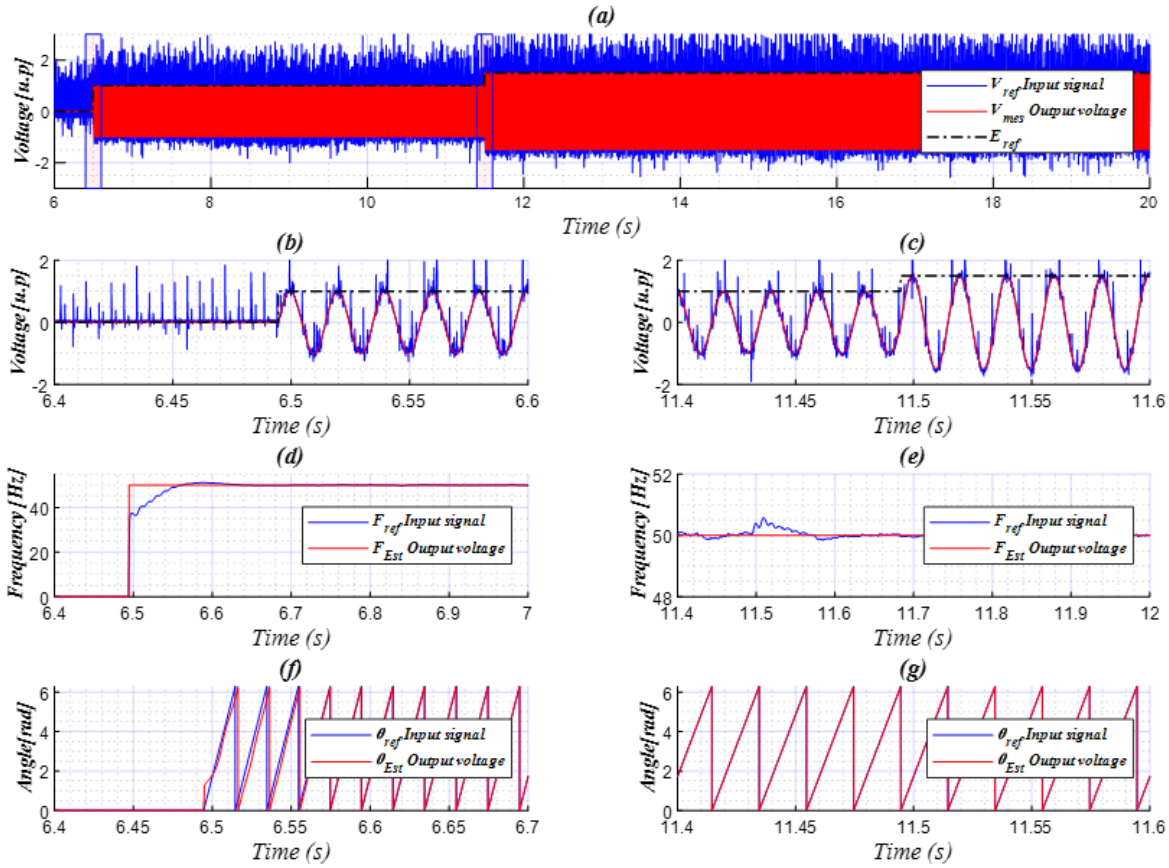


Fig. 3.14. *Experimental results for amplitude step change.*

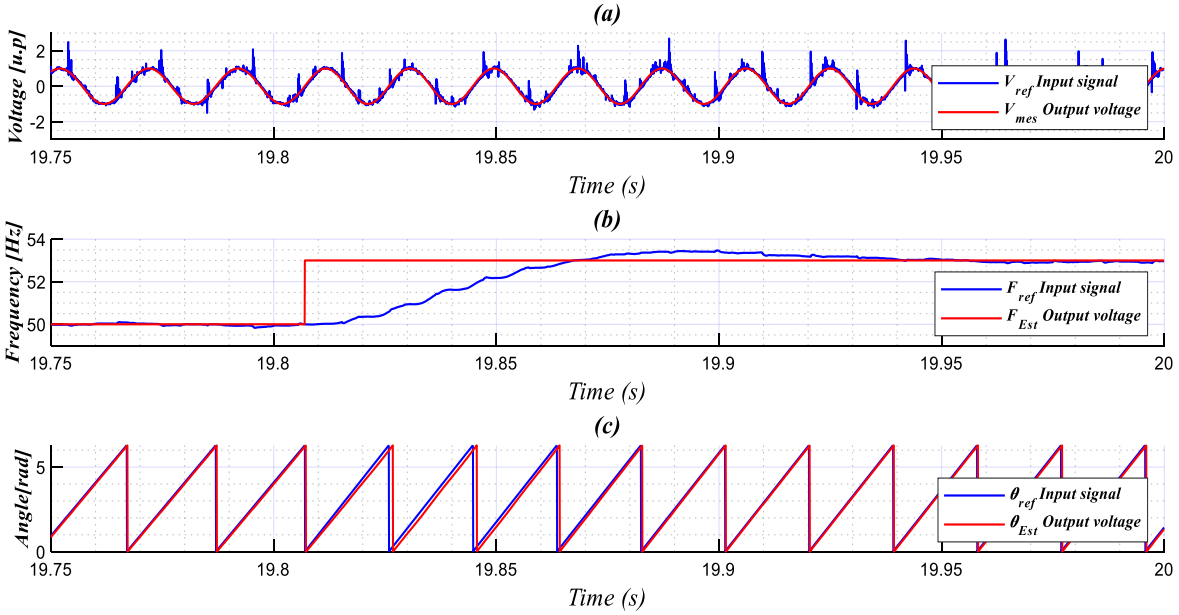


Fig. 3.15. *Obtained experimental results in response to frequency change.*

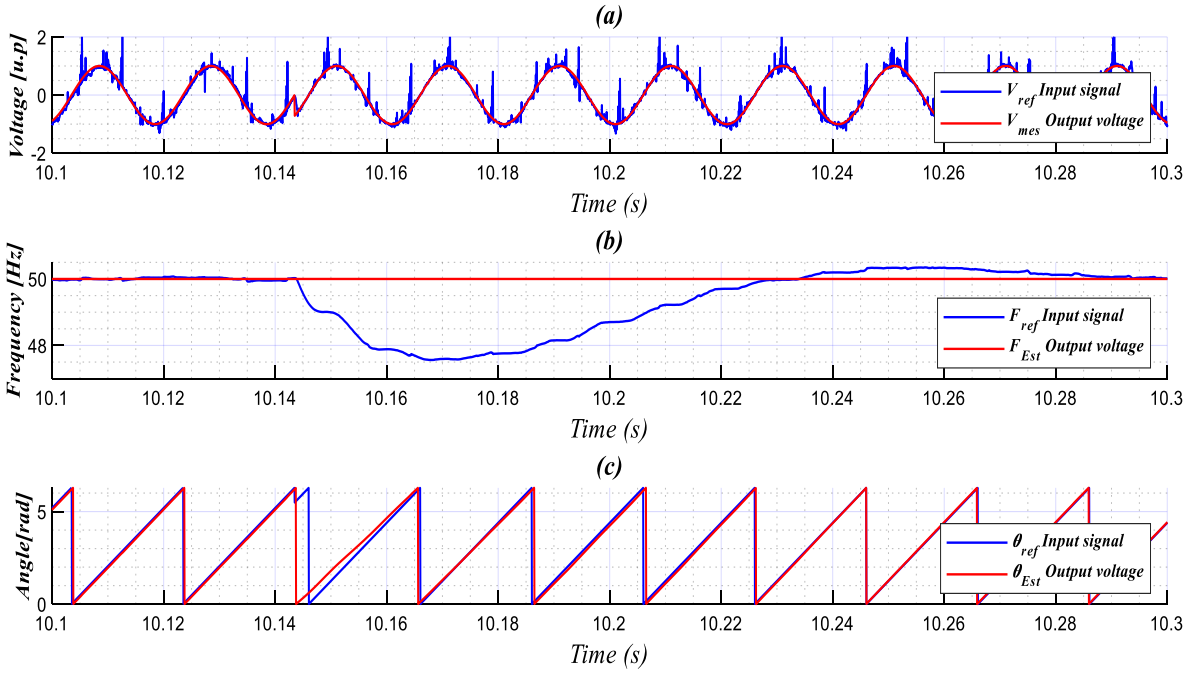


Fig. 3.16. *Obtained experimental results for angle phase jump.*

3.8 Conclusion

In this chapter, the design, modeling and analysis of the inner control loops for single-phase VSI-interfaced MG has presented. The design of a dual-loop inner control includes a current control loop based on P controller and an IP-type-based voltage control loop has proposed. The modeling of the current and voltage control loops has developed, and the respective closed-loop models have obtained. A guideline for proper tune of the controllers' parameters by using the obtained model has described. The stability of the LC-filtered VSI system incorporating current and voltage control loops has analyzed. The robustness of the designed controller to voltage reference change and system parameter variations has assessed. Simulations have performed using MATLAB/Simulink environment, to verify the effectiveness of the designed controller. In addition, experimental tests have carried out to confirm the performances of the control purpose. The obtained simulation and experimental results have shown the performance of the designed controller in achieving improved transient response with fast settling time and without overshoots under different conditions. This means that the inner controllers can track perfectly, accurately and quickly the voltage and current references, therefore, they may lead to improvement of the performance of the whole microgrid control.

Chapter IV:

Improved Power Sharing Control for Droop-Controlled Single-Phase VSIs in Standalone Microgrid Considering Nonlinear Load Operation

Chapter IV:

Improved Power Sharing Control for Droop-Controlled Single-Phase VSIs in Standalone Microgrid Considering Nonlinear Load Operation

In this chapter, the development of an improved power sharing control scheme for droop-operated single-phase VSIs in standalone MG is presented. The proposed control scheme includes an enhanced active and reactive power calculation unit and a frequency-adaptive virtual impedance loop. The detailed analysis of the two proposed units involved in the power-sharing scheme is provided in this chapter. Besides, the chapter presents an investigation of the performance of these units as well as of the whole proposed power-sharing controller.

4.1 Introduction

Microgrid primary control, as a local controller, is the first control level that should be established in order to guarantee load sharing between parallelized VSIs during the autonomous operating mode [12], [122]. This control level is usually based on the droop control method, which uses only local-measured information and no need for intercommunication signals between the inverters [123], [124]. Such a method introduces proportional droops in the voltage frequency and amplitude references of the inverter according to the active and reactive powers, respectively, demanded by the load [125]. These powers are generally calculated by using a power calculation block included in the primary control layer. In this regard, the calculation of the power is a crucial aspect, since the stability and performance of droop-based control are strongly influenced by its speed and accuracy, especially in the case of nonlinear loads [126]. Further, an additional important aspect in such a control system is the virtual output impedance, which is introduced to improve the power-sharing accuracy among VSIs, regardless of line impedance unbalances and the sharing of nonlinear loads [127]. This aspect has, also, a critical influence on power-sharing based control accuracy and stability.

Traditional calculation methods for single-phase droop-controlled systems compute the instantaneous active and reactive powers by the multiplications of the inverter measured output current with the inverter output voltage, and with its 90° phase-shifted version [128]; created by a quarter-cycle delay unit. In such methods, a low-pass filter (LPF) which is imperative, is used to remove the double frequency components result from the product of the output current with

output voltage components and achieving the perspective average active and reactive powers. Other methods introduced additional quarter-cycle delay units to handle the double frequency components cancellation [67, 86], [129]. Instead of using delay units and to avoid its issues; strict limitations on achievable feedback performance [71]; advanced methods based on the SOGI scheme for power computation intended for single-phase system, have been proposed [130–132]. These methods use the SOGI as an estimator of the voltage and current components as well as the double frequency components estimation/rejection. The method presented in [130], calculates the instantaneous powers similar to the conventional method, but it introduces two SOGI blocks to extract the oscillating components at twice of the fundamental frequency to be substrate from the instantaneous powers. In [131], an approach uses the SOGI to estimate the filtered direct and quadrature components of the inverter output voltage. The direct product of these voltage components with the output current is performed, and the double frequency components cancellation based on SOGI is adopted for achieving the average active and reactive powers. Other methods introduce the SOGI to extract the direct and quadrature components of both output voltage and current has been handled in [132]. Then, these components are employed to calculate the average powers in the $\alpha\beta$-frame, similarly to the three-phase instantaneous *PQ* theory. These power calculation methods based on SOGI can be easily implemented and without delay as well as they have the advantages of fast transient response and accepted rejection capability of load distortions. Nevertheless, LPF is still necessary for such as methods to proper rejection of harmonics under worst voltage distortions. However, the LPF limits the transient response speed of the power calculation and degrading the power-sharing stability, especially under nonlinear load conditions, where its cutoff frequency should be reduced even more to minimize the distortions induced in the inverter output current. In regard to avoiding the use of LPF, solutions based on the discrete Fourier transform (DFT) and a Least Mean Squares (LMS) approach for achieving the average active and reactive powers, have been presented in [69] and [70]. These methods have the main drawback is that both of them need more computation time to perform P/Q calculations. In addition, a particular drawback for the DFT based method is that it introduces a significant time delay in the system process. Furthermore, the LMS based-method has a poor dynamic response regarding the overshoot term.

In general, all the aforementioned methods have not properly taken into consideration the case of nonlinear load conditions and undesirable output voltage and current inherent disturbances, then, power calculation with good performance cannot be guarantee. DC component, which may be caused by MG faults, conversion process, and measurement devices, is one of the major disturbances that may affect the performance of these methods, worsening the stability of the parallelized system.

For these reasons, recent approaches have been proposed in the literature to overcome this issue and ensure fast and accurate calculation of average powers while considering nonlinear loads. These methods are designed by introducing an advanced SOGI-based scheme suitable for DC offset and nonlinear load harmonic rejection capability [133]. For instance, the power calculation method based on the DSOGI strategy is presented in [71]. This method is similar to [132], but it introduces the DSOGI to estimate perfectly filtered direct fundamental component of the output current by ensuring the high rejection of the DC component and current distortions. This component is multiplied by the voltage fundamental extracted by using standard SOGI, and the average powers are obtained after removing the double frequency component. Roughly speaking, in case of the presence of the DC component in the inverter voltage, the performance of this method might be questionable due to the sensibility of the SOGI to such as disturbance [133]. In [73], an approach for power calculation is proposed by using the n-SOGI strategy, which is applied to extract the orthogonal fundamental components of both inverter output voltage and current. Then, these components are used to calculate the voltage amplitude and phase, then, the active and reactive power can be obtained by exploiting sine and cosine functions. Despite this method have provided performance enhancement of power calculation under the DC component and nonlinear load conditions, it needs more computational time due to the use of the trigonometric functions, therefore, a control with high computation burden is expected.

Regarding the virtual impedance, various approaches-based droop control schemes have been addressed in the literature aiming to achieve accuracy in harmonics load sharing between VSIs [134–137]. However, since the virtual impedance control loop takes as input the inverter output current, their performance can be affected by the output-current inherent noise and nonlinear load distortions. Therefore, virtual impedance implementation based on the SOGI scheme has been proposed in [77] and [138]. In this method, virtual impedance is implemented by using the outputs of the SOGI, v_α, and v_β, considering inductive, resistive, and complex impedances. The method has less sensitive to the output current noise, achieves output-voltage total harmonic distortion, and enhances the sharing of nonlinear loads. Another concept for the implementation of virtual impedance by using MSOGI strategy has been developed in [80], to regulate the virtual impedance at the fundamental frequency, and virtual impedance at selected harmonic frequencies. Although, the presented methods have improved the sharing of current harmonics, especially the last one, the presence of the DC component in the output current can affect the SOGI and MSOGI performance, hence, the virtual impedance control. To deal with this issue, the TOGI algorithm, which can cancel the DC component and its effects, has been adopted in [79], to implement the virtual impedance. Nevertheless, the method considered only the fundamental virtual impedance, without considering harmonic virtual impedances, hence, proper harmonics current sharing cannot

be guarantee.

In regard to all aforementioned issues, the authors in the present work aim to improve the performance of the power-sharing among single-phase droop-controlled VSIs in islanded microgrid considering DC component and nonlinear load disturbances. To achieve this goal, a improved power-sharing scheme includes a Multiple Enhanced SOGI-FLL-based proposed power calculation approach, and frequency-adaptive virtual impedance loop is developed. The MESOGI-FLL strategy can provide high rejection capability of DC component and current harmonics, hence, perfect estimation of the output current fundamental component of the inverter and its 90◦ phase-shifted version, which are required for power calculation. This strategy makes the power calculation method-based control scheme immune to disturbance effects of the DC component and the nonlinear current harmonics. A description of a conventional method, advanced and recent power calculation methods are provided. Also, detailed analysis is provided, mathematical model of the MESOGI, that cannot be found in the literature, is derived, and a simulation study evaluating the performance of the proposed power calculation method in comparison to the recent methods is performed. On the other side, an adaptive virtual impedance control loop is, also, considered in the developed scheme for the aim of improving the load harmonics sharing. This control loop exploits the outputs of the MESOGI-FLL, i.e., i_α, i_β, and its 3, 5, and 7 versions of the output current, to calculate the virtual impedance output voltage. The proposed control scheme can guarantee an accurate share of the active and reactive power between parallel-connected VSIs regardless of the load condition. In addition, it can provide a robust operation of the MG system when VSIs shared nonlinear loads. Furthermore, since only one MESOGI-FLL block is required for the current components' estimation in both units, therefore, contributes to minimizing the computational time of the whole implemented control. Simulation and experimental tests are performed and the obtained results show the effectiveness, robustness of the proposed power-sharing controller even under nonlinear load operating conditions.

4.2 Proposed Power Sharing Control Scheme for Droop-Operated Single-Phase VSIs

In a single-phase microgrid, each distributed generation unit operating in parallel has an independent local controller, named the primary control layer. In this control layer, the droop control method is generally employed to ensure power-sharing between VSIs. **Fig. 4.1**, shows a schematic diagram of the proposed power-sharing approach-based primary control scheme for a single-phase VSI in islanded MG. In the designed power-sharing block, as seen, an enhanced power calculation method based on MESOGI-FLL is introduced to provide accurate averaged powers. These powers are entered into the droop-controller for generating the frequency and

amplitude references. These generated references are processed by a sinusoidal signal generator to provide the fundamental component reference of the inverter's output voltage. Meanwhile, a frequency-adaptive virtual-impedance loop is involved to provide the expected voltage of the virtual output impedance. This unit uses the same MESOGI-FLL block to extract the in-phase and the orthogonal components as well as its harmonics components for computing the virtual impedance voltage, to be added to the fundamental output voltage reference given by the droop control. The new delivered voltage reference is manipulated by a multi-loop inner controller and a PWM to command the inverter's switches.

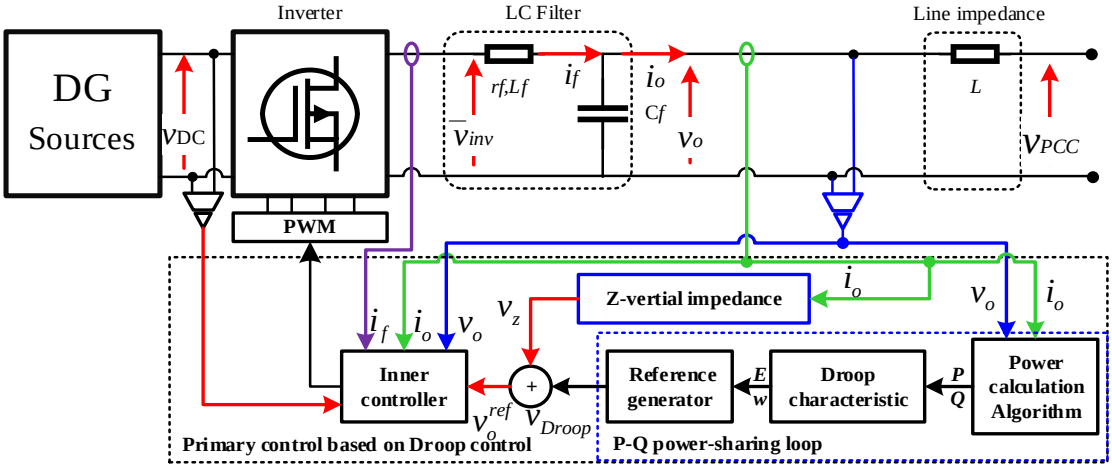


Fig. 4.1. *The proposed power-sharing approach-based primary control for a single-phase inverter.*

The use of the MESOGI-FLL strategy, that characterizes by its good transient response, precise estimation of the current fundamental components as well as perfect estimation/rejection of the current harmonic components and DC component, as an estimator, may enhance the performance of both power calculation and virtual impedance units. As a result, it may improve the performance of the power-sharing based on droop control in both transient and steady-state, even in case of nonlinear load distortions and the presence of DC component in the inverter outputs. Furthermore, notice that the same MESOGI-FLL is used for the two units, hence, the computational time may be minimized.

Aiming to examine the performance of the designed power-sharing control scheme, analysis of the proposed power calculation method and the frequency-adaptive virtual impedance unit are investigated in what came. Note that the main focus is given to the proposed power calculation method which considered our novelty. Accordingly, an overview of conventional, advanced, and recent methods intended for power calculation-based power sharing control in single-phase MG is explored in the following sections. In addition, the proposed power calculation scheme based

on the MESOGI-FLL technique and corresponding mathematical analysis are inspected. Moreover, a comparative study between the two recent methods and the proposed one regarding the performance of the power calculation is conducted. Description and analysis of an adaptive virtual impedance control loop use the outputs of the MESOGI-FLL are also presented.

4.3 Overview of Power Calculation methods for single-phase microgrid

In this section, a study of several conventional and advanced methods, as well as recent methods for power calculation in single-phase droop-controlled VSI are investigated.

4.3.1 Conventional and Advanced Power calculation methods

A conventional method and two advanced methods for the power calculation are described in this subsection; transfer delay- and SOGI-QSG-based power calculators.

a) Transfer Delay-based power calculation method

The schematic diagram of the conventional *P*-*Q* calculation method based on a time-delay unit is depicted in **Fig. 4.2** [71]. As seen in this figure, the instantaneous active power is calculated by multiplying the direct version of the output voltage and current. Then, filtering the instantaneous power p_i by a low-pass filter (LPF), with a low and a fixed cut off frequency value, to get the average value of the active power P. Similarly, the average reactive power can be obtained by only introducing a quarter-period delay (i. e., 90° phase-shift) of the output voltage.

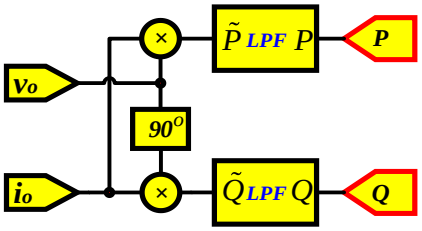


Fig. 4.2. *The structure of power calculation based on the low-pass filter.*

As mentioned in [73], the LPF with very low cut-off frequency is needed to reject the undesirable oscillating components at twice of the fundamental frequency and the distortions induced by current harmonics in case of nonlinear loads. However, the use of such as LPF may slow down the velocity of the estimated powers transient response, hence, it may decrease the droop control performance. Moreover, an erroneous estimation of the 90° phase-shift version of the output voltage is expected due to the use of a fixed quarter-period delay (f_n/4), especially, in the case of the droop method-based control scheme, where the operating frequency f_{droop} is varying according to the load change (i. e., $f_{droop} = f_n \pm 50$).

b) Advanced Power calculation methods using SOGI for generating the orthogonal component

To overcome the undesired delay and the double frequency ripple component issues, two methods based on SOGI-QSG are adopted [77], [138]. In this method, the SOGI-QSG is mainly included to extract the orthogonal component from a single-phase output voltage.

Fig. 4.3 shows the block diagram of the first method, which includes a SOGI-QSG with FLL as an adaptive estimator for estimating filtered in-phase and in-quadrature phase components of the inverter output voltage. Accordingly, the instantaneous active and reactive powers are determined by proceeding the product of the extracted voltage components and the measured output current of the inverter. Another two SOGI-QSG units are integrated to capture the powers ripples at twice of the fundamental frequency to be substrate from the instantaneous powers. These SOGI-QSG units are tuned both at $2\hat{\omega}$ and $\xi_1 = \xi_2 = 0.7$. LPF is integrated to filter out the harmonics and provide the averaged active and reactive powers.

The structure of the second method for power calculation based on SOGI-FLL is illustrated in **Fig. 4.4**. In this structure, two SOGI-QSG blocks, which are both tuned at the estimated fundamental frequency of the input signal by the FLL detector, are used to extract the inverter output current and voltage, direct and quadrature fundamental components ($v_{\alpha,\beta,}$ and $i_{\alpha,\beta}$). Hence, the average active and reactive powers (P and Q) can be calculated in $\alpha\beta$-frame, by using the extracted current and voltage components, according to the expressions given by **Eq. (4.1)**, below. Additionally, an LPF is involved to provide more harmonics rejection capabilities.

$$\begin{cases} P = \dfrac{1}{2}\left(v_d i_d + v_q i_q\right) \\ Q = \dfrac{1}{2}\left(v_q i_d - v_d i_q\right) \end{cases} \tag{4.1}$$

where the subscripts α and β denotes the direct and quadrature components of the output voltage/current of inverter in the $\alpha\beta$-stationary reference frame.

Despite the presented methods has the ability to cancel the pulsating double frequency power components and offer good harmonics rejection, they still suffer from the LPF issues in slowing down the speed of the system transient response. Furthermore, the presence of the DC component in the inverter output current and voltage is the main disturbance that may affect the performance of both given methods.

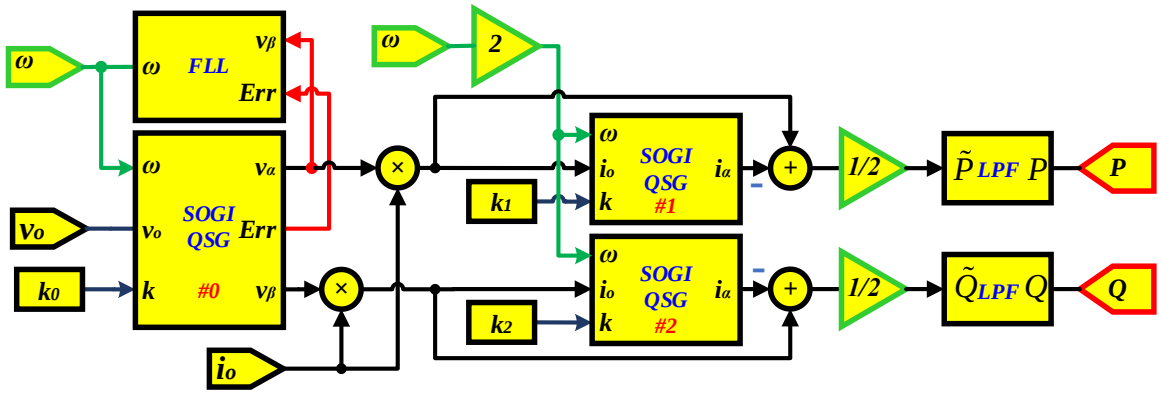


Fig. 4.3. Structure of the P-Q calculation scheme using an additional SOGI for generating the -π/2 delay [138].

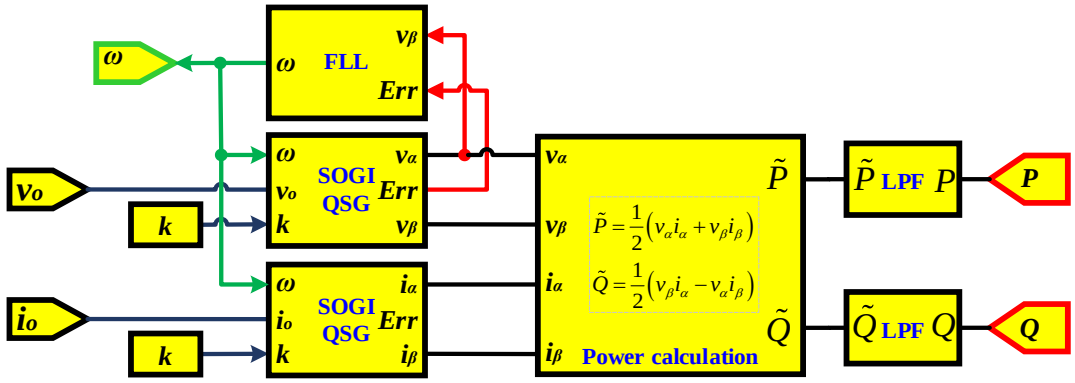


Fig. 4.4. The structure of the power calculation method based on the SOGI-FLL for producing the current and voltage orthogonal components.

In fact, the SOGI-FLL is highly sensitive to the presence of dc component and it may cause fundamental-frequency oscillatory errors in the output of the SOGI-QSG. Consequently, these issues can affect the performance of the power calculation-based power sharing control system.

4.3.2 Recent power calculation methods

This section describes the recent methods intended for improving the power calculation performance considering DC component and nonlinear distortions in the output current. These methods introduce additional cascaded SOGI-QSGs to filter out the undesirable disturbances that may inherent in the inverter output signals instead of using LPF.

a) P-Q calculation method based on DSOGI-QSG

Fig. 4.5, illustrates the LPF-less power calculation method that consists in a modification of **Fig. 4.3**. According to **Fig. 4.3**, an additional DSOGI-QSG block, tuned at ω, is integrated to offer

high rejection of the DC offset and nonlinear harmonic distortions. This block takes as an input, the output current of the inverter, to estimate a filtered direct component i_α corresponding to the fundamental frequency. The instantaneous active p and reactive q powers are computed, similar to the method given by **Fig. 4.5**, by using the estimated filtered direct component and the fundamental components, provided by the SOGI-FLL, of the inverter current and voltage, respectively. Then, the respective averaged powers are obtained after filtering out the double frequency ripple component.

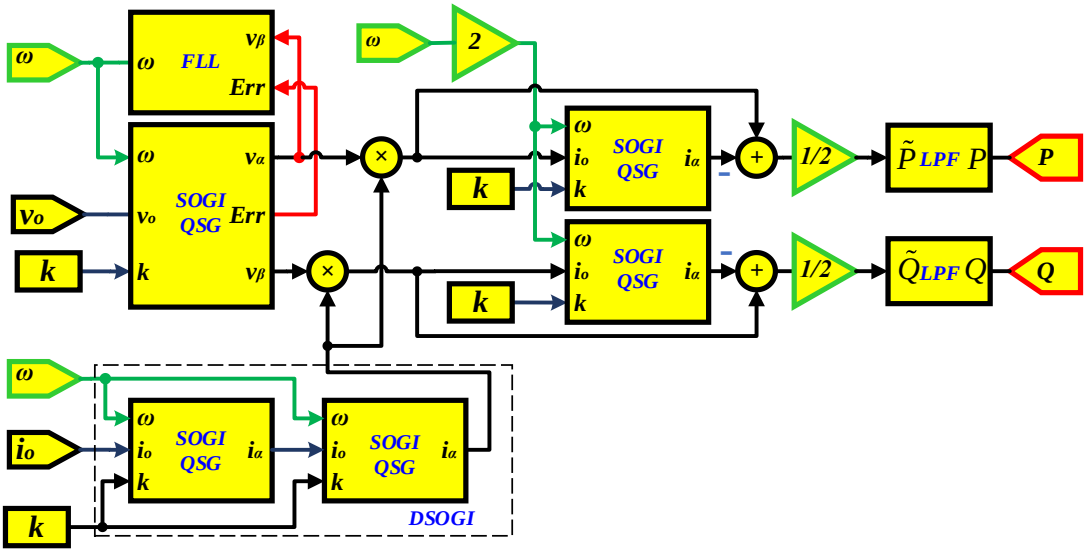


Fig. 4.5. Structure of the P-Q calculation method based on DSOGI-QSG.

The performance of the presented power calculation based-scheme may improve in terms of transient response and sub-harmonic and harmonic rejection capabilities regarding the current component estimation. But, regarding the voltage estimation, the problem of SOGI-FLL sensitivity to disturbance effects of the DC component that probably present in the inverter voltage, as mentioned earlier, is still present. This may decrease the control performance when the output voltage contains a DC component as it is may degrade the stability of the overall system.

b) Power Calculation Method considering n-Order SOGI Filtering

The recent method for calculating the average value of the active and reactive powers developed by [73] is given in **Fig. 4.6 (a)**. The main idea of the presented method is to provide an estimation of the current and voltage fundamental components with high filtering performance by using the n-order cascaded SOGI-QSG (n-SOGI) technique. The estimated fundamental components are used to calculate the amplitude and angle-phase of the inverter voltage and current. Hence, the averaged active and reactive powers (P and Q) can be computed according to the expressions of the fundamental powers, mentioned in standard IEEE-1954-2010, defined as

follow:

$$\hat{P} = \frac{1}{2}|\hat{v}_o||\hat{i}_o|\sin\left(\theta_{v_o} - \theta_{i_o}\right)$$
$$\hat{Q} = \frac{1}{2}|\hat{v}_o||\hat{i}_o|\cos\left(\theta_{v_o} - \theta_{i_o}\right) \quad (4.2)$$

being the amplitude and angle phase estimations of the voltage and the current fundamental components, respectively. These parameters can be expressed by the following mathematical formulations:

$$\begin{cases} |v_o| = \sqrt{v_\alpha^2 + v_\beta^2} \\ |i_o| = \sqrt{i_\alpha^2 + i_\beta^2} \end{cases}, \quad \begin{cases} \theta_{v_o} = Arctg\left(\dfrac{v_\beta}{v_\alpha}\right) \\ \theta_{i_o} = Arctg\left(\dfrac{i_\beta}{i_\alpha}\right) \end{cases} \quad (4.3)$$

where the symbol $|\ |$ denote the amplitude and the symbols θ_{v_o} and θ_{i_o} denote the angle phase.

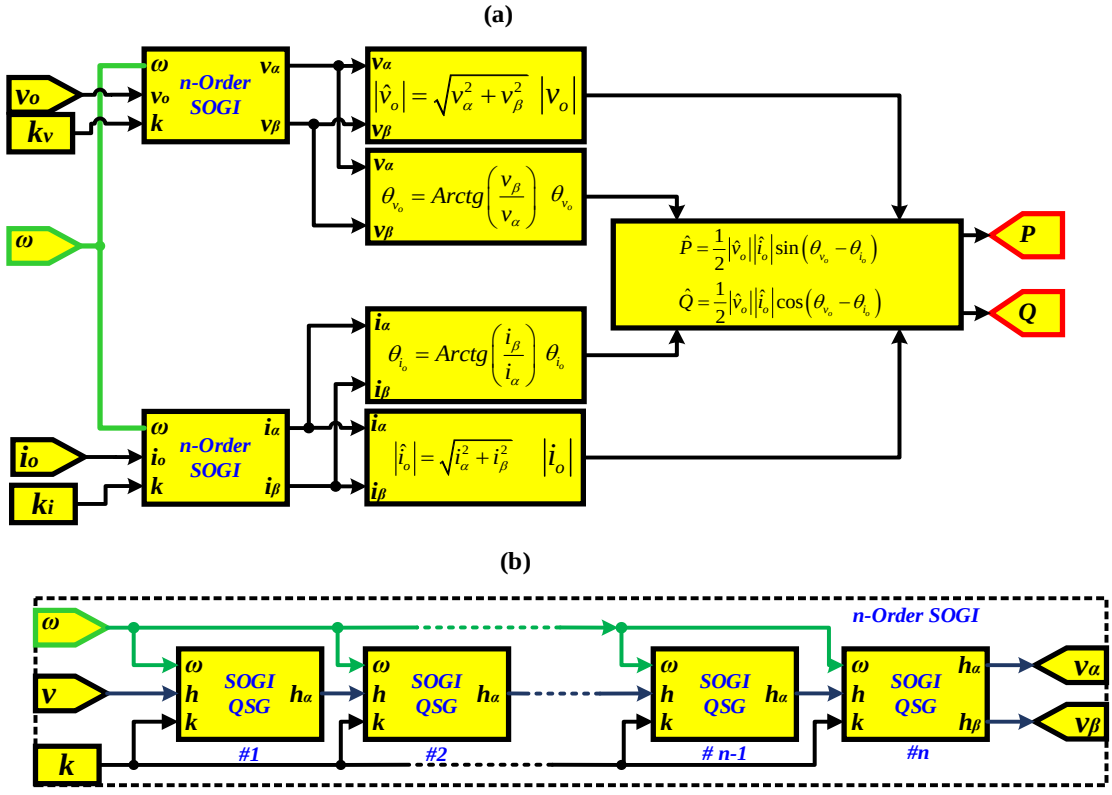


Fig. 4.6. Schematic diagram depicting; ***(a)*** *the recent P and Q calculation method based on n-SOGI structure;* ***(b)*** *the scheme of cascaded n-order SOGI-QSG.*

As depicted in **Fig. 4.6 (b)**, the n-SOGI-QSG composes of #n unit of the SOGI-QSG associated in cascade. These SOGI-QSG blocks are tuned at the fundamental frequency ω.

It is worth noting that this method does not require additional SOGI units for rejecting the ripple of the double frequency components.

By using the n-Order SOGI method, the DC component, sub-harmonics, and harmonic distortions are totally rejected from both current and voltage. Thus, it leads to proper and accurate calculation of the *P* and *Q* powers under any disturbances and nonlinear operating conditions. As a result, the presented method can contribute to improving the performance of the power calculation-based droop control scheme as well as deal with the drawbacks of all the aforementioned methods. The fact is the presented method process sine, cosine, and tangent functions computation, which may significantly increase the computation time, hence, getting a high computation burden control implementation [133]. To this sense, the need for an improved method for power calculation which can provide a tradeoff between accuracy and performance, i. e., fast dynamic response, high disturbances rejection, and implementation simplicity is mandatory. This is the main focus of the authors in the next section, where an effective fast and accurate method of averaged power calculations is proposed taking into consideration the DC component and nonlinear load disturbances.

4.4 Proposed enhanced power calculation method

This section deals with the design, modeling, and analysis of a proposed power calculation method based on the MESOGI-FLL scheme for single-phase droop-operated VSIs. **Fig. 4.7** shows the structure of the proposed method, which consists of; i) a MESOGI-QSG approach apply to extract accurately the direct and the quadrature fundamental components as well as its 3, 5, and 7 harmonic versions, of the inverter output current; ii) an Enhanced SOGI-QSG method (ESOGI-FLL) suitable for DC offset rejection, uses for estimating the fundamental components of the inverter voltage; iii) FLL unit adapts the center frequency of both MESOGI and ESOGI to frequency changes. The estimated fundamental components of the inverter voltage and current are exploited to calculate the averaged active and reactive powers in the $\alpha\beta$-frame. By the way, the MESOGI can offer a fast estimation of the current components with high DC component and harmonic rejection capabilities from this current under non-linear load conditions, and the ESOGI regarding the voltage components estimation as well. Hence, the proposed approach can ensure fast and accurate average active and reactive power calculation with good transient performance even in the case of highly distorted current. In addition, as the MESOGI-FLL, which does not process any trigonometric functions, can be easily implemented, it contributes to reducing the power calculation computation time and as a result, getting low computational burden power-sharing control.

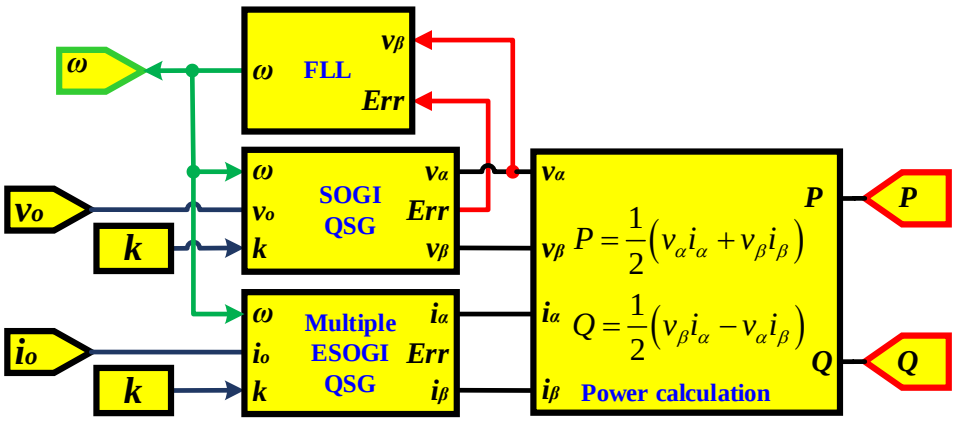


Fig. 4.7. Schematic diagram of the proposed power calculation method based on MSOGI-FLL.

In the next section, a detailed description of the proposed MESOGI-QSG is given. Also, as the model of the MSOGI-QSG estimations has yet been derived, the modeling procedure for obtaining the dynamic model of the MESOGI-FLL regarding v_α, v_β, and V_{dc} estimation, is developed. Obtaining such a mathematical model requires to facilitate the MESOGI-QSG analysis as well as its performance enhancement, as will be shown.

4.4.1 Multiple ESOGI-QSG modeling and analysis

4.4.1.1 Structure of the MESOGI-QSG

Fig. 4.8 (a) shows the Multiple-ESOGI-QSG structure adopted to estimate precisely the current components under very extreme distortion conditions (DC component and nonlinear load). This proposed structure includes n ESOGI-QSG adaptive suitable for DC component rejection, given in **Fig. 4.8 (b)**, connected in parallel. The involved ESOGI-QSG is formed by adding a rejection/estimation unit (LPF) to the standard SOGI-QSG (see **Fig. 4.8 (b)**). This ESOGI-QSG provides total rejection of the DC component as well as its effect from the output components [133]. Each ESOGI-QSG adaptive filter, in the proposed structure, is tuned to a different frequency multiple of the fundamental frequency, by multiplying the fundamental frequency estimated by the FLL by a coefficient that determines the order of the harmonic assigned. Furthermore, the gain *k* of each ESOGI-QSG is divided by the order such coefficient in order to maintain a constant relationship between fundamental frequency and the bandwidth of the SOGI-QSG. The input current for each ESOGI-QSG is calculated by subtracting all the rest of the in-phase output components of the other ESOGI-QSG from the actual input current.

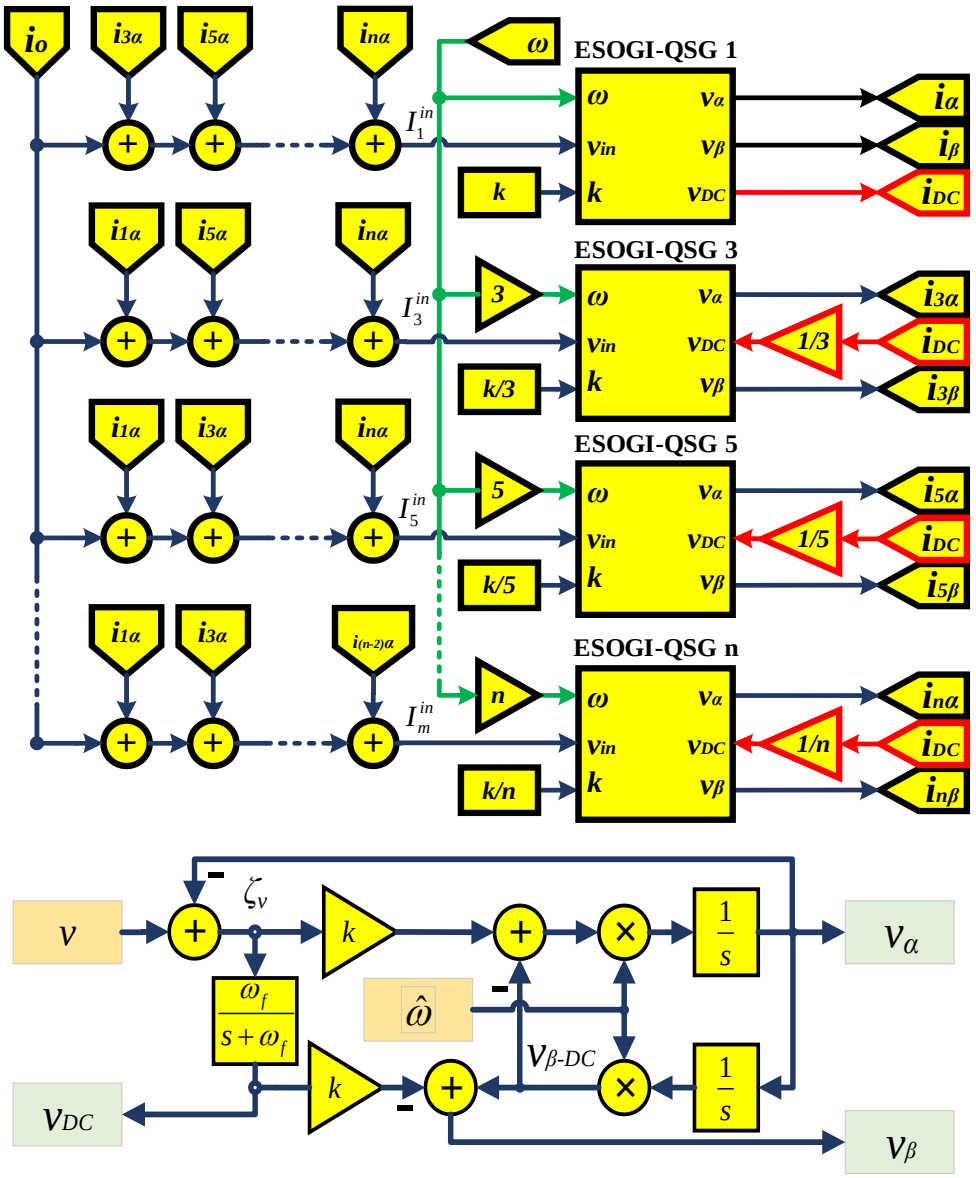


*Fig. 4.8. Structure of; **(a)** the MESOGI-FLL method and **(b)** the ESOGI method.*

In this regard, the input current of each SOGI-QSG is cleaned up, after a transient process, from the harmonic components estimated by the rest of SOGI-QSGs, which will reject the harmonic distortions at its output.

4.4.1.2 MESOGI-QSG modeling

According to the structure given in **Fig. 4.8**, the transfer functions of the outputs ($i_{\alpha-n}$, $i_{\beta-n}$ and i_{DC}) of the ESOGI-QSG units can be given by the following expressions:

$$\begin{cases} i_{\alpha-n} = G_{\alpha-n} i_n^{in} \\ i_{\beta-n} = G_{\beta-n} i_n^{in} - (k/n) i_{DC} \\ i_{DC} = G_{DC} \left(i_1^{in} - i_{1-\alpha} \right) \end{cases} \quad (4.4)$$

where

$$\begin{cases} G_{\alpha-n} = \dfrac{i_{\alpha-n}}{i_n^{in}} = \dfrac{k\,\omega s}{s^2 + k\,\omega s + n^2\omega^2} \\ G_{\beta-n} = \dfrac{i_{\beta-n-DC}}{i_n^{in}} = \dfrac{kn\omega^2}{s^2 + k\,\omega s + n^2\omega^2} \\ G_{DC} = \dfrac{i_{DC}}{i_1^{in} - i_{\alpha-1}} = \dfrac{\omega_f}{s + \omega_f} \end{cases} \tag{4.5}$$

In addition, from this figure, the equation of the input current i_n^{in} of each ESOGI-QSG block with the input signal i_o can be written as follows:

$$i_j^{in} = i_o - \sum_{\substack{p=0 \\ i=2p+1 \\ i\neq j}}^{n} i_{\alpha-i} \tag{4.6}$$

Eq. (4.6) can be written as a matrix as follows:

$$\begin{bmatrix} i_1 \\ i_3 \\ i_5 \\ \vdots \\ i_n \end{bmatrix}^{in} = -\begin{bmatrix} 0 & 1 & 1 & \cdots & 1 \\ 1 & 0 & 1 & \cdots & 1 \\ 1 & 1 & 0 & \cdots & 1 \\ \vdots & \vdots & 1 & \ddots & \vdots \\ 1 & 1 & 1 & \cdots & 0 \end{bmatrix} \begin{bmatrix} i_{\alpha-1} \\ i_{\alpha-3} \\ i_{\alpha-5} \\ \vdots \\ i_{\alpha-n} \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} i_o \tag{4.7}$$

Based on **Eq. (4.4)**, the transfer functions of the output components of the ESOGI-QSG adaptive filter blocks can be represented in matrix form as follows:

a- For the output components $i_{\alpha-n}$, which is, in-phase with the input signal i_n^{in} of each ESOGI-QSG block

$$\begin{bmatrix} i_{\alpha-1} \\ i_{\alpha-3} \\ i_{\alpha-5} \\ \vdots \\ i_{\alpha-n} \end{bmatrix} = \begin{bmatrix} G_{\alpha-1} & 0 & 0 & \cdots & 0 \\ 0 & G_{\alpha-3} & 0 & \cdots & 0 \\ 0 & 0 & G_{\alpha-5} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & G_{\alpha-n} \end{bmatrix} \begin{bmatrix} i_1 \\ i_3 \\ i_5 \\ \vdots \\ i_n \end{bmatrix}^{in} \tag{4.8}$$

b- For the output components $i_{\beta-n}$, which is, quadrature-phase with the input signal i_n^{in} of each ESOGI-QSG block

$$\begin{bmatrix} i_{\beta-1} \\ i_{\beta-3} \\ i_{\beta-5} \\ \vdots \\ i_{\beta-n} \end{bmatrix} = \begin{bmatrix} G_{\beta-1} & 0 & 0 & \cdots & 0 \\ 0 & G_{\beta-3} & 0 & \cdots & 0 \\ 0 & 0 & G_{\beta-5} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & G_{\beta-n} \end{bmatrix} \begin{bmatrix} i_1 \\ i_3 \\ i_5 \\ \vdots \\ i_n \end{bmatrix}^{in} - \begin{bmatrix} k \\ k/3 \\ k/5 \\ \vdots \\ k/n \end{bmatrix} i_{DC} \tag{4.9}$$

c- For the output components i_{DC}, which is, the dc-component with the input signal i_n^{in} and the output components $i_{\alpha-n}$of each ESOGI-QSG block.

$$i_{DC} = G_{DC}[1 \quad 0 \quad 0 \quad \cdots \quad 0]\left(\begin{bmatrix} i_1 \\ i_3 \\ i_5 \\ \vdots \\ i_n \end{bmatrix}^{in} - \begin{bmatrix} i_{\alpha-1} \\ i_{\alpha-3} \\ i_{\alpha-5} \\ \vdots \\ i_{\alpha-n} \end{bmatrix}\right) \tag{4.10}$$

By substituting **Eq. (4.7)** in **Eqs. (4.8)** to **(4.10)**, the closed-loop transfer functions of the output components of the proposed structure can be expressed as follows:

a- For the output components $i_{\alpha-n}$

$$\begin{bmatrix} i_{\alpha-1} \\ i_{\alpha-3} \\ i_{\alpha-5} \\ \vdots \\ i_{\alpha-n} \end{bmatrix} = \begin{bmatrix} 1 & G_{\alpha-1} & G_{\alpha-1} & \cdots & G_{\alpha-1} \\ G_{\alpha-3} & 1 & G_{\alpha-3} & \cdots & G_{\alpha-3} \\ G_{\alpha-5} & G_{\alpha-5} & 1 & \cdots & G_{\alpha-5} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ G_{\alpha-n} & G_{\alpha-n} & G_{\alpha-n} & \cdots & 1 \end{bmatrix}^{-1} \begin{bmatrix} G_{\alpha-1} \\ G_{\alpha-3} \\ G_{\alpha-5} \\ \vdots \\ G_{\alpha-n} \end{bmatrix} i_o \tag{4.11}$$

b- For the output components $i_{\beta-n}$

$$\begin{bmatrix} i_{\beta-1} \\ i_{\beta-3} \\ i_{\beta-5} \\ \vdots \\ i_{\beta-n} \end{bmatrix} = \left(- \begin{bmatrix} 0 & G_{\beta-1} & G_{\beta-1} & \cdots & G_{\beta-1} \\ G_{\beta-3} & 0 & G_{\beta-3} & \cdots & G_{\beta-3} \\ G_{\beta-5} & G_{\beta-5} & 0 & \cdots & G_{\beta-5} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ G_{\beta-n} & G_{\beta-n} & G_{\beta-n} & \cdots & 0 \end{bmatrix} \begin{bmatrix} 1 & G_{\alpha-1} & G_{\alpha-1} & \cdots & G_{\alpha-1} \\ G_{\alpha-3} & 1 & G_{\alpha-3} & \cdots & G_{\alpha-3} \\ G_{\alpha-5} & G_{\alpha-5} & 1 & \cdots & G_{\alpha-5} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ G_{\alpha-n} & G_{\alpha-n} & G_{\alpha-n} & \cdots & 1 \end{bmatrix}^{-1} \begin{bmatrix} G_{\alpha-1} \\ G_{\alpha-3} \\ G_{\alpha-5} \\ \vdots \\ G_{\alpha-n} \end{bmatrix} + \begin{bmatrix} G_{\beta-1} \\ G_{\beta-3} \\ G_{\beta-5} \\ \vdots \\ G_{\beta-n} \end{bmatrix} \right) i_o - \begin{bmatrix} k \\ k/3 \\ k/5 \\ \vdots \\ k/n \end{bmatrix} i_{DC} \tag{4.12}$$

c- For the output component i_{DC}

$$i_{DC} = G_{DC}\left(1 - [1 \quad 1 \quad 1 \quad \cdots \quad 1] \begin{bmatrix} 1 & G_{\alpha-1} & G_{\alpha-1} & \cdots & G_{\alpha-1} \\ G_{\alpha-3} & 1 & G_{\alpha-3} & \cdots & G_{\alpha-3} \\ G_{\alpha-5} & G_{\alpha-5} & 1 & \cdots & G_{\alpha-5} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ G_{\alpha-n} & G_{\alpha-n} & G_{\alpha-n} & \cdots & 1 \end{bmatrix}^{-1} \begin{bmatrix} G_{\alpha-1} \\ G_{\alpha-3} \\ G_{\alpha-5} \\ \vdots \\ G_{\alpha-n} \end{bmatrix}\right) i_o \tag{4.13}$$

As it is well known, the distortions of the near harmonics from the fundamental component (i.e., 3, 5, and 7 harmonics) have a big effect on the output fundamental components than the distortions of the high harmonics (far from the fundamental component). Therefore, only the 3^{rd}, 5^{th}, and 7^{th} low harmonics are taken into consideration in our study, where they will be estimated/rejected from the input fundamental signal of the proposed MESOGI-FLL structure.

Accordingly, the closed-loop transfer functions of the proposed structure regarding the estimation of the output components $i_{\alpha-n}$ and $i_{\beta-n}$ corresponding to the fundamental component, the selected 3^{rd}, 5^{th}, and 7^{th} harmonics, and the DC component can be expressed as follows:

a- For the output components $[i_{\alpha-1}, i_{\alpha-3}, i_{\alpha-5}, i_{\alpha-7}]^T$

$$\begin{bmatrix} i_{\alpha-1} \\ i_{\alpha-3} \\ i_{\alpha-5} \\ i_{\alpha-7} \end{bmatrix} = \begin{bmatrix} G_{BF.\alpha-1} \\ G_{BF.\alpha-3} \\ G_{BF.\alpha-5} \\ G_{BF.\alpha-7} \end{bmatrix} i_o \tag{4.14}$$

b- For the output components $\left[i_{\beta-1}, i_{\beta-3}, i_{\beta-5}, i_{\beta-7}\right]^T$

$$\begin{bmatrix} i_{\beta-1} \\ i_{\beta-3} \\ i_{\beta-5} \\ i_{\beta-7} \end{bmatrix} = \begin{bmatrix} G_{BF.\beta-1} \\ G_{BF.\beta-3} \\ G_{BF.\beta-5} \\ G_{BF.\beta-7} \end{bmatrix} i_o \tag{4.15}$$

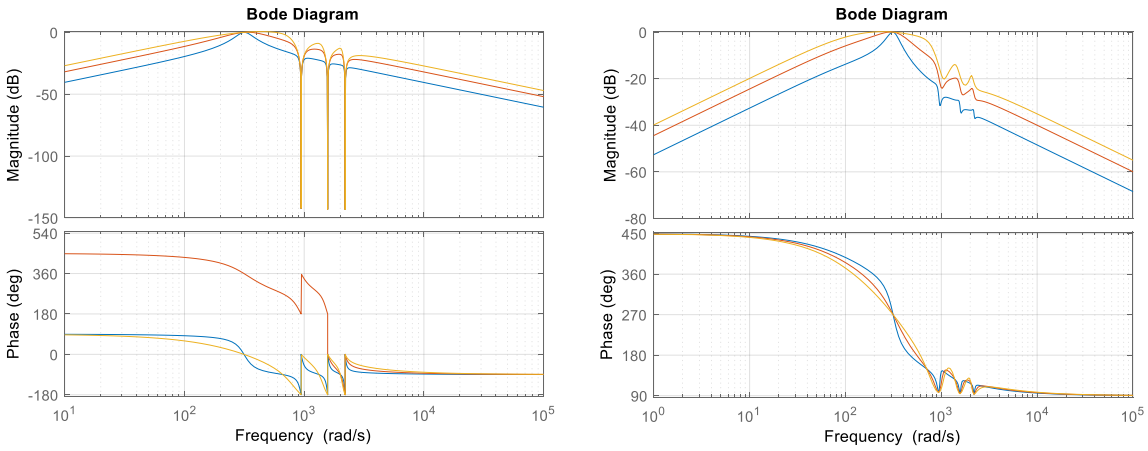
c- For the output component i_{DC}

$$i_{DC} = G_{BF.DC}.i_o \tag{4.16}$$

while the $G_{BF.\alpha-1,3,5,7}$ and $G_{BF.\beta-1,3,5,7}$, are the transfer functions relating the output components to the input current (i_o), and their expressions will be given in appendix I.

The magnitude and phase bode plots of the closed-loop transfer functions $G_{BF.\alpha-1,3,5,7}$ and $G_{BF.\beta-1,3,5,7}$ of the 1^{st}, 3^{rd}, 5^{th}, and 7^{th} harmonics are depicted in **Fig. 4.9 (a)**, **(b)**, **(c)**, and **(d)**, respectively. The frequency response curves; of $G_{BF.\alpha-1,3,5,7}$ and $G_{BF.\beta-1,3,5,7}$; are presented for three different values of the damping factor, k = 0.3,0.7, and sqrt (2), and for $\omega = 2\pi\times50$ (rad/s). According to these figures, it can be observed that the transfer functions $G_{BF.\alpha-1,3,5,7}$ and $G_{BF.\beta-1,3,5,7}$ exhibit band-pass adaptive filters, which their bandwidth depends on the gain k. As can be seen, increasing k decreases the filter bandwidth, hence, enhance the filtering capabilities of the sub-harmonics (i. e., 3, 5 and 7 harmonics). But, this effect slowdowns the speed of the estimates' transient response.

(a)



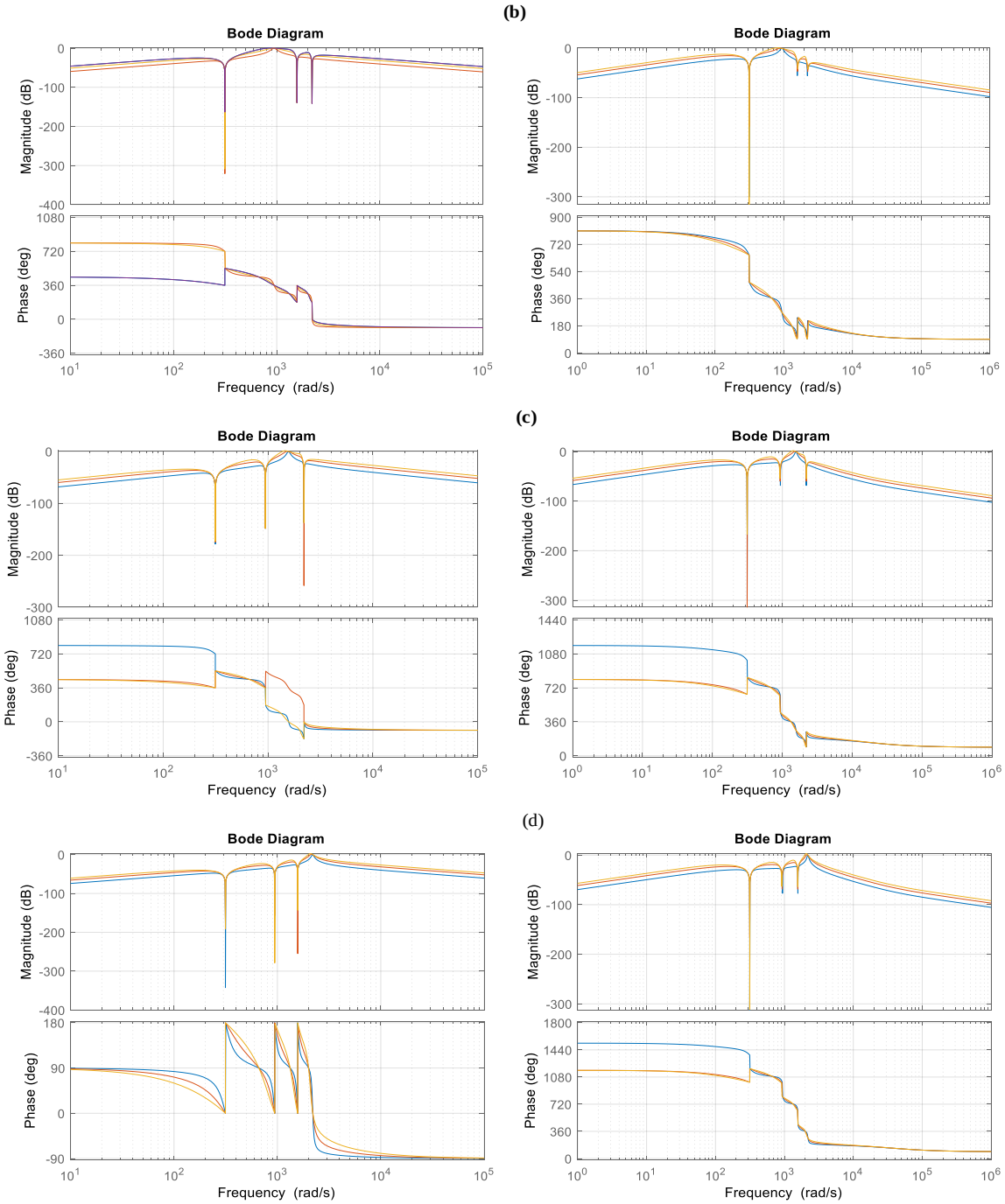


Fig. 4.9. *The frequency response of the proposed MESOGI-FLL structure regarding the direct and orthogonal output components estimation* ***(a)*** *fundamental harmonic,* ***(b)*** *3 harmonic,* ***(c)*** *5 harmonic, and* ***(d)*** *7 harmonic.*

Further, from these figures, one can be noticed that the output components $i_{\alpha-1}, i_{\alpha-3}, i_{\alpha-5}, i_{\alpha-7}$ have the same amplitude and synchronize in the phase with the harmonics set in the input signal (i_o). Similarly, the output components $i_{\beta-1}, i_{\beta-3}, i_{\beta-5}, i_{\beta-7}$ have the same amplitude and quadrature in the phase with the harmonics set in the input signal (i_o).

As a consequence, the proposed MESOGI-FLL can ensure proper estimation of the direct and

quadrature fundamental components, as well as provides good estimation/rejection of the 3, 5, and 7 harmonic and DC components.

4.5 Comparative study

In order to examine the performance of the power calculation based on the proposed method in comparison with the other presented methods, a simulation study is conducted in the MATLAB environment. In this study, the performance of the proposed strategy and the other methods are evaluated in front of input current and voltage perturbations (without and with DC component and harmonic distortions). The simulations are performed corresponding to the following tests:

Test 1: In this test, no sub-harmonic and harmonic distortions are induced in the input current and voltage expressed by **Eq. (4.17)**, below. This test is conducted in the response to an amplitude step change of the inverter current from the peak of 0A to 5A.

$$\begin{cases} v_o = V \times \sin(\omega t) \\ i_o = I \times \sin(\omega t - \varphi) \end{cases} \quad (4.17)$$

Test 2: DC component and harmonic distortions are introduced in the input current and voltage as following, respectively:

- DC component with 2%, 10% of the third-harmonic, 5% of the fifth-harmonic, and 1% of the seventh-harmonic form amplitude of the input current (i_o);
- 2 % of DC component, 50% of the 3rd harmonic, 10% of the 5th harmonic, and 5% of the 7th harmonic form amplitude of the input voltage (v_o);

Accordingly, the mathematical expressions of v_o and i_o can be given as follow:

$$\begin{cases} v_o = 0.02V + V \times \sin(\omega t) + 0.1V \times \sin(3\omega t) + 0.05V \times \sin(5\omega t) + 0.01V \times \sin(7\omega t) \\ i_o = 0.02I + I \times \sin(\omega t - \varphi) + 0.5I \times \sin(3\omega t - \varphi) + 0.1I \times \sin(5\omega t - \varphi) + 0.05I \times \sin(7\omega t - \varphi) \end{cases} \quad (4.18)$$

The parameters for the simulated schemes, in this comparative study, are described in ***Table 4.1***.

The obtained results of this comparative study in response to tests 1 and 2 are illustrated in **Fig. 4.10** and **Fig. 4.11**, respectively. They show the *P* and *Q* calculation performance obtained by the proposed method are compared with those provided by the other methods-based scheme, for input current step change. Based on these simulation results the following remarks can be made.

Table 4.1. *Parameters of the power calculation methods*

Method	Block	Parameters	Symbol	Unit	Value
Proposed Method	ESOGI-QSG, Multiple- ESOGI-QSG, MFLL	SOGI-QSG gain	Z	-	0.6
		FLL gain	Γ	s^{-1}	50
		LPF cut-off frequency	$\omega_f / 2\pi$	Hz	20
Add-SOGI	SOGI-QSG #0, FLL	SOGI-QSG gain	k_0	-	1
		FLL gain	Γ	s^{-1}	50
	SOGI-QSG #1,2	SOGI-QSG gain	$k_{1,2}$	-	0.707
	LPF	cut-off frequency	$\omega_c / 2\pi$	Hz	10
SOGI	SOGI-QSG, FLL	SOGI-QSG gain	k	-	0.7
		FLL gain	Γ	s^{-1}	50
	LPF	cut-off frequency	$\omega_c / 2\pi$	Hz	10
DSOGI	DSOGI-QSG	SOGI-QSG gain	k	-	0.21
n-Order SOGI	n-SOGI-QSG FLL	SOGI-QSG gain	k_v	-	0.7
		SOGI-QSG gain	k_i	-	0.25
		FLL gain	Γ	s^{-1}	50

For test 1 :

- All the power calculation structures have the same steady-state responses, in which no ripples can be noticed in the estimated active and reactive power.

- The SOGI-based *P* and *Q* calculation method has the fastest transient response but with significant oscillations, whereas, the method-based DSOGI has the slowest transient response but without any oscillations (very small oscillations in the calculated Q).

- The scheme based on Add-SOGI can achieve the *P* and *Q* calculation with good transient response behavior but with a high settling time, after the one based on DSOGI.

- The proposed scheme is faster calculating the *P* and *Q* than the other method, except the one-based SOGI, and without oscillations in the transient response.

For test 2 :

- The performance of the power computation (P and Q) using the SOGI- and n-SOGI-based scheme are much affected by the induced DC component and harmonics into the input current and voltage, in which they suffer from suffers from higher ripple distortion at steady-state and large oscillations in the transient response are obtained.

- The features of the structure based on the DSOGI regarding active power calculation is not influenced by the introduced perturbations, where, a less ripple distortions than all the other methods are observed (with small oscillations can be noticed in the Q calculation transient response). Despite, these features, this method has a very slow dynamic response.

- The proposed scheme and the scheme based on Add-SOGI have very close improved performances in terms of DC component and harmonics effects rejection in the estimated P and Q. as seen much lower ripple than the first two methods are obtained. However, the proposed scheme has better settling time than this method (Add-SOGI) and

n-SOGI and DSOGI-based scheme as well.

- It is worth noting that further oscillations are obtained in the estimated reactive power of all methods.

As a consequence, one can be deduced that the proposed scheme can achieve better power calculation performance in term of speed of dynamic response, high DC component and harmonics rejection capabilities (almost no ripples at steady-state), and very low oscillation in the transient response, than all the other methods.

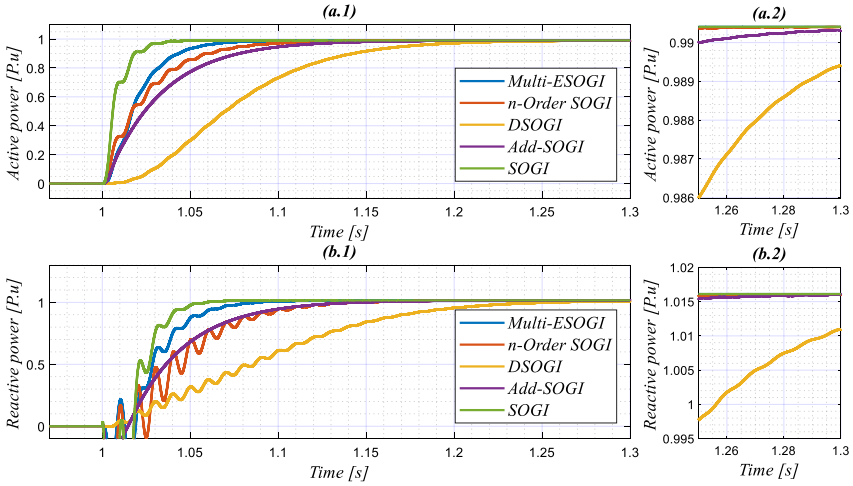


Fig. 4.10. *Obtained results in response to Test 1,* ***(a)*** *active power, and* ***(b)*** *reactive power.*

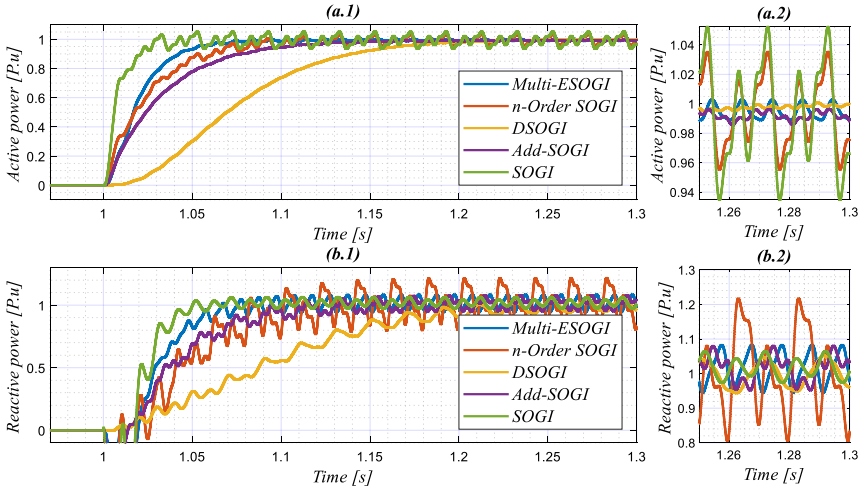


Fig. 4.11. *Obtained results in response to Test 2,* ***(a)*** *active power, and* ***(b)*** *reactive power.*

4.6 Frequency-adaptive virtual-impedance control loop

For the sake of enhancing the droop control performances in terms of current harmonics sharing when feeding nonlinear loads, a frequency-adaptive virtual-impedance loop is proposed based on Multiple ESOGI-QSG. In this purpose, the outputs of Multi ESOGI-FLL, i. e., fundamental direct component, quadrature component and its versions corresponding to 3, 5 and

7 harmonics are used to calculate the expected virtual-impedance voltage v_z, as shown in **Fig. 4.12**. The proposed scheme can offer a precise and accurate calculation of the virtual-impedance voltage, to be added to the voltage reference generated by droop control and providing the new voltage reference, that can be expressed by:

$$v^{ref}(s) = v^{ref}_{droop}(s) - z_v(s) i_o(s) \tag{4.19}$$

where the $z_v(s)$ is the virtual-output impedance.

According to **Fig. 4.12**, the expression of virtual impedance voltage as a function of fundamental and harmonics components of the output current can be derived as follows:

$$v_z(s) = r_v i_o - L_v \hat{\omega}\left(i_{\beta-1} + 3i_{\beta-3} + 5i_{\beta-5} + 7i_{\beta-7}\right) \tag{4.20}$$

being $\boldsymbol{r_v}$ and $\boldsymbol{L_v}$ the virtual-output resistance and inductance, respectively.

By using **Eq. (4.15), Eq. (4.20)** can be written, in matrix from, as follows:

$$v_z(s) = r_v i_o - L_v \hat{\omega}\begin{bmatrix}1 & 3 & 5 & 7\end{bmatrix}\begin{bmatrix} i_{\beta-1} \\ i_{\beta-3} \\ i_{\beta-5} \\ i_{\beta-7}\end{bmatrix} = \left(r_v - L_v \hat{\omega}\begin{bmatrix}1 & 3 & 5 & 7\end{bmatrix}\begin{bmatrix} G_{BF.\beta-1} \\ G_{BF.\beta-3} \\ G_{BF.\beta-5} \\ G_{BF.\beta-7}\end{bmatrix}\right) i_o \tag{4.21}$$

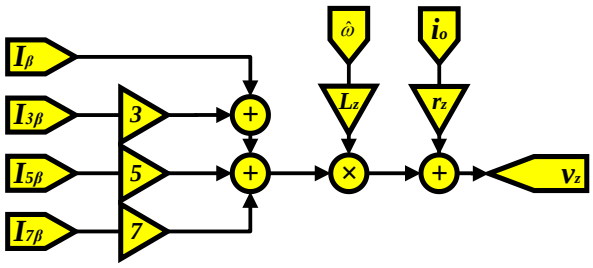


Fig. 4.12. *Simplified diagram of virtual-impedance implementation based on MESOGI.*

Consequently, the virtual-output impedance expression can be derived as follows:

$$z_v(s) = r_v - L_v \hat{\omega}\begin{bmatrix}1 & 3 & 5 & 7\end{bmatrix}\begin{bmatrix} G_{BF.\beta-1} \\ G_{BF.\beta-3} \\ G_{BF.\beta-5} \\ G_{BF.\beta-7}\end{bmatrix} \tag{4.22}$$

4.6.1 Analysis of the output-impedance considering the virtual-impedance

Based on **Fig. 4.13 (a)**, that depict the Thevenin equivalent circuit of a VSI with a voltage

control loop, which represented by an AC voltage source with a low output-impedance in series [14], the expression of the voltage control closed-loop can be given by **Eq. (4.23)** below. Accordingly, the expression of the voltage closed -loop considering the virtual impedance loop, can be derived as given in **Eq. (4.24)**.

$$v_o = \left[G_{vo-vo}(s)\right] v_{droop}^{ref} - \left[z_o(s)\right] i_o \tag{4.23}$$

$$v_o = \left[G_{vo-vo}(s)\right].v_{droop}^{ref} - \left[G_{vo-vo}(s).z_v(s) + z_o(s)\right] i_o \tag{4.24}$$

where $\boldsymbol{z_o(s)}$ is the transfer function of the equivalent output-impedance of the VSI with the control loop in Laplace-domain, that can be written as follows:

$$z_o(s) = G_{vo.io}(s) \tag{4.25}$$

being $G_{vo.io}(s)$ the transfer function relating the output voltage to the output current of the VSI, and its expression was given in **chapter 3** by **Eq. (3.14)**.

The Thevenin equivalent circuit of the VSI with voltage control and virtual impedance loops is shown in **Fig. 4.13 (b)**.

According to **Eq. (4.24)**, the expression of the equivalent output-impedance after integrated the new voltage reference, **Eq. (4.19)**, can be concluded, which is writing as follows:

$$z_G = G_{vo-vo}(s).z_v(s) + z_o(s) \tag{4.26}$$

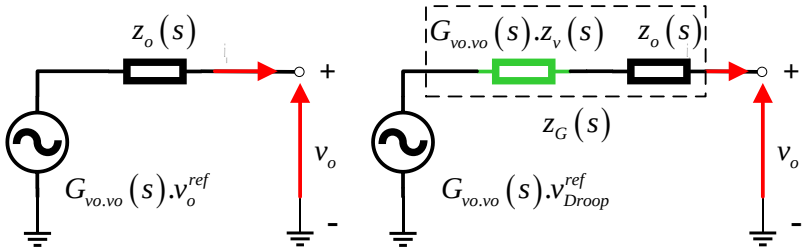
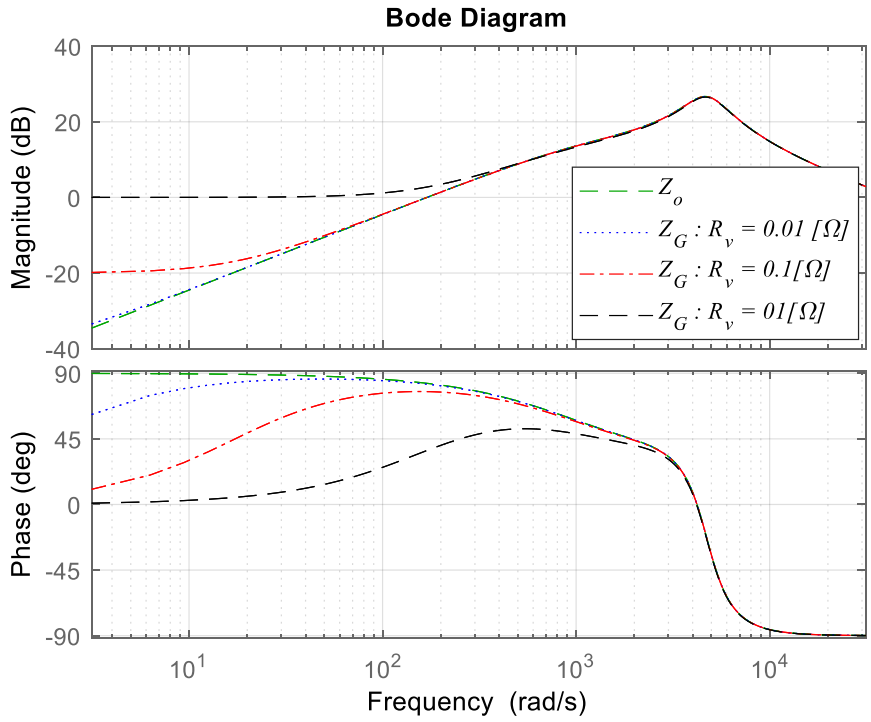


*Fig. 4.13. Thevenin equivalent circuit of a voltage controlled-VSI; **(a)** without, and **(b)** with virtual-impedance.*

To study the impact of the virtual-impedance into the output-impedance as well as selecting properly the values of the virtual-output resistance and inductance, frequency analysis is presented. The Bode diagram of the transfer function of the output-impedances z_o and z_G (with virtual-impedance) for three different values of the virtual resistance (r_v) and the inductance (L_v) are presented in **Fig. 4.14 (a)** and **(b)**, respectively.

(a)



(b)

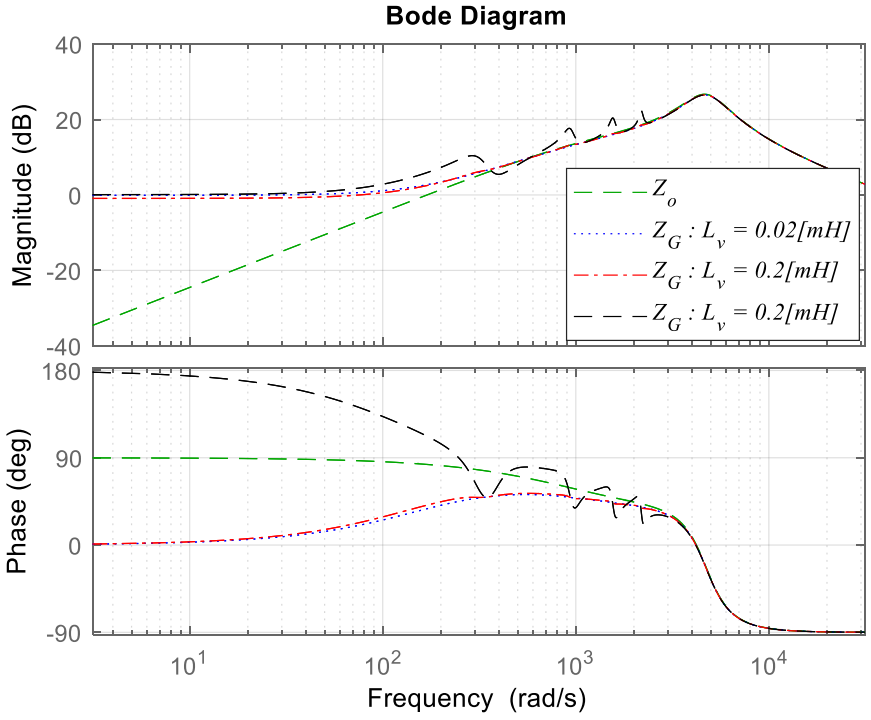


Fig. 4.14. *Frequency response of the output impedance z_o and z_G, (a) $r_v = \{0.01\Omega, 0.1\Omega, 1\Omega\}$, $L_v = 0$, and (b) $L_v = \{0.02mH, 0.2mH, 2mH\}$, $r_v = 1\Omega$.*

As can be seen in **Fig. 4.14 (a)**, when increasing the virtual resistance, the output impedance z_G behavior changes from inductive to resistive with an increase in its amplitude for low frequencies. In addition, it is clearly shown that output impedance (z_G) behavior for the high

harmonics does not change regarding z_o, no matter how the resistance r_v value changes.

From **Fig. 4.14 (b)**, it can be observed that the amplitude amount of the output impedance (z_G) at the selective harmonics increase when increasing the value of the virtual inductive. Also, it is illustrated that the behavior of output impedance z_G at the low frequencies is a variable resistor no matter how the inductance L_v value changes. Further, the output impedance (z_G) behavior of the high harmonics does not change regarding z_o, no matter how the inductance L_v value changes.

According to the presented analysis, one can be concluded that the increase in both inductance L_v and the resistance r_v increase the value of the output impedance z_G in comparison to the output impedance z_o, this effect leads to reducing the impact of the line-impedance unbalances.

4.7 Simulation Results

In this section, numerical tests are performed in order to assess the effectiveness of the proposed power-sharing control. In these tests, the performance of the proposed control scheme is verified in the case of sharing linear and nonlinear and during linear load change as well. The testbed considered in the simulations is depicted in **Fig. 4.15**, and it consists of two single-phase parallel-connected inverters connected to a common AC bus through line impedance. These inverters supply a critical load and formed islanded microgrid. The microgrid system with the proposed control scheme is simulated in the Sim Power Systems under the MATLAB/Simulink environment. The proposed power-sharing control stage is as given in **Fig. 4.1**, which comprises the improved power calculation and adaptive virtual impedance units.

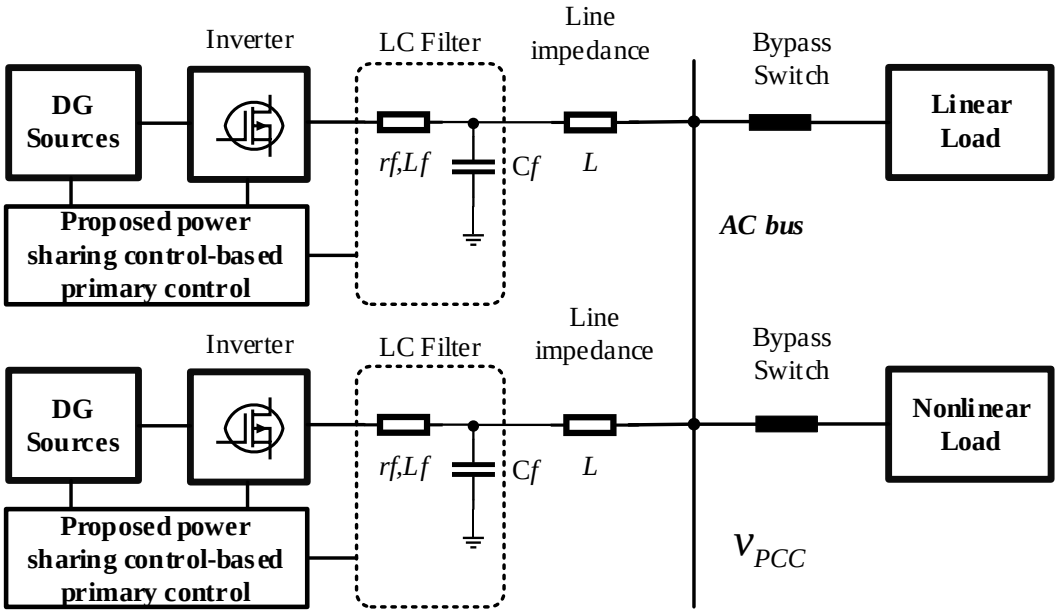


Fig. 4.15. simulated model of the two DG units interfaced microgrid in MATLAB/simulink.

The main parameters taken the simulations are given in **Table 4.2**, **Table 4.3**. Notice that a Gaussian noise is added to DC voltage sources and sensors' measures.

Fig. 4.16 illustrates the preformed scenarios for the connection and disconnection of linear load1 and load2. The obtained results in response to linear load change are shown in **Fig. 4.17, Fig 4.18,** and **Figs. 4.19.** In these figures, the time responses of the active and reactive power, output voltage amplitude, and frequency, as well as the output voltage and current waveforms of inverters 1 and 2 are presented. First, there is no load connected to the MG, the inverter frequencies and amplitudes are equal and set to their nominal values i. e., $f_{DG1} = f_{DG1} = f_n$ and $E_{DG1} = E_{DG2} = E_n$), while P_{DG1}, P_{DG2}, Q_{DG1} and Q_{DG2} powers are equal to zero. After, when the first load is connected (at t = 1 s), the inverters active and reactive powers increase and the output voltage frequencies (f_{DG1} and f_{DG1}) and amplitudes (E_{DG1} and E_{DG2}) droop, as seen in **Fig. 4.17**. At t = 2 s, the second load is added, the powers seamlessly increase without overshot and with reduced settling time (0.02 s). In addition, the amplitudes, E_{DG1} and E_{DG2}, and the frequencies, f_{DG1}, and f_{DG1}, droop even more with the same amount, and with a faster dynamic response. Further, it can be noticed that the active power is perfectly shared among the inverters. The same observation can be made for the rest of the scenarios, when the first and the second loads, disconnected and connected again.

According to **Fig. 4.18** and **Figs. 4.19**, one can be observed that the inverters output voltages, $\boldsymbol{v_{o\text{-}DG1}}$ and $\boldsymbol{v_{o\text{-}DG2}}$, are matched, as well as the currents, $\boldsymbol{i_{o\text{-}DG1}}$ and $\boldsymbol{i_{o\text{-}DG2}}$, and have pure sinusoidal forms, also, they change with good transient responses during linear load variations.

The results showing the performance of the proposed controller when the inverters shared nonlinear load are presented in **Fig. 4.21, Fig. 4.22** and **Fig. 4.23**, while **Fig. 4.20** presents the performed scenarios. The nonlinear load is represented by a full-bridge diode rectifier with resistive loads. **Fig. 4.21, Fig. 4.22,** and **Fig. 4.23** depict the time evolution of the same variables of test 1. Similar to test 1, the MG system starts with the no-load operation, then, at t = 1 s a nonlinear load is connected to the MG. As seen in **Fig. 4.21**, the VSIs active powers grow and have the same values which means that they share accurately the load power demand. Also, these powers achieve the rated values respective to load demand, with a fast response time of 0.02 s and without overshoots, and they do not have any ripple distortions or oscillating components in steady-state, even with the distorted currents, as can be seen in **Fig. 4.22 and Fig. 4.23**. Further, the figures demonstrate that $\boldsymbol{f_{DG1}}$ and $\boldsymbol{f_{DG1}}$ droop with the same amounts, showing excellent dynamic response in terms of settling time (0.02 s) and without oscillations, and no ripples are obtained in steady-state as well. Regarding the voltage amplitudes, it can be observed that they

increase to compensate the load reactive powers, which is shared between the two VSIs. From the output voltage and current, in this case, shown in **Fig. 4.22** and **Fig. 4.23**, one can be noted that the inverters' voltages, $v_{o\text{-}DG1}$ and $v_{o\text{-}DG2}$, are matched and have sinusoidal waveforms, while the currents are equal and take the nonlinear load current form to compensate the load reactive power. Moreover, it is clearly appearing those transient responses with good performance are obtained.

Table 4.2. *Parameters of the simulation study*

Parameters	Symbol	Unit	Value
Nominal Voltage	E_n	V	220
Nominal frequency	f_n	Hz	50
Switching frequency	f_s	kHz	20
Simulation frequency	f_s	MHz	1
DC voltage	U_{DC}	V	495
Output filter capacitor	C	µF	23
Output filter inductor	L,r	mH, Ω	2, 1
Line impedance of DG #1	L_1	mH, Ω	1.5, 0.8
Line impedance of DG #2	L_2	mH, Ω	0.5, 0.8
Virtual inductance	L_v	mH	2.7
Virtual Resistance	R_v	Ω	1
P-ω droop	m	-	0.0005
Q-*V* droop	n	-	0.001
Voltage controller P gain	k_{pv}	-	0.1839
Voltage controller I gain	k_{pi}	-	183.87
Current controller P gain	k_{iv}	-	6.2831

Table 4.3. *Sensors' variance*

Parameters	Value
voltage sensors	22.5
Current sensors	0.3

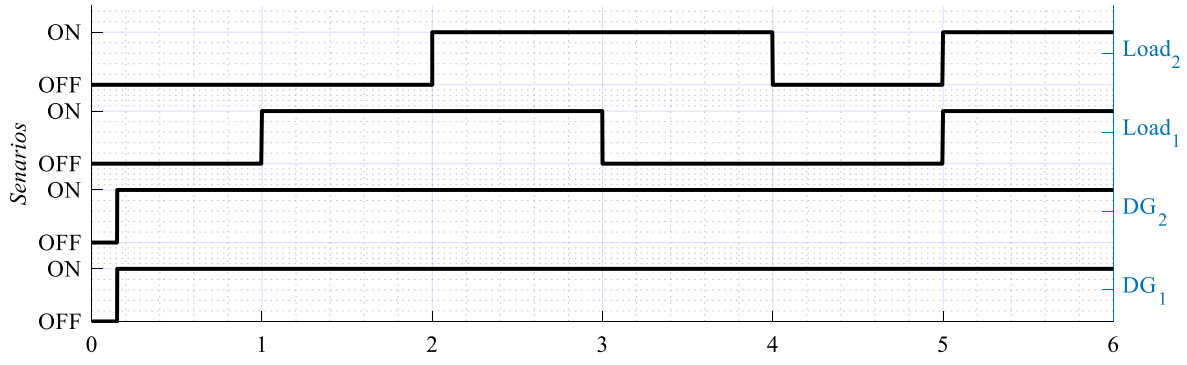


Fig. 4.16. *Plots of the performed scenarios for test 1.*

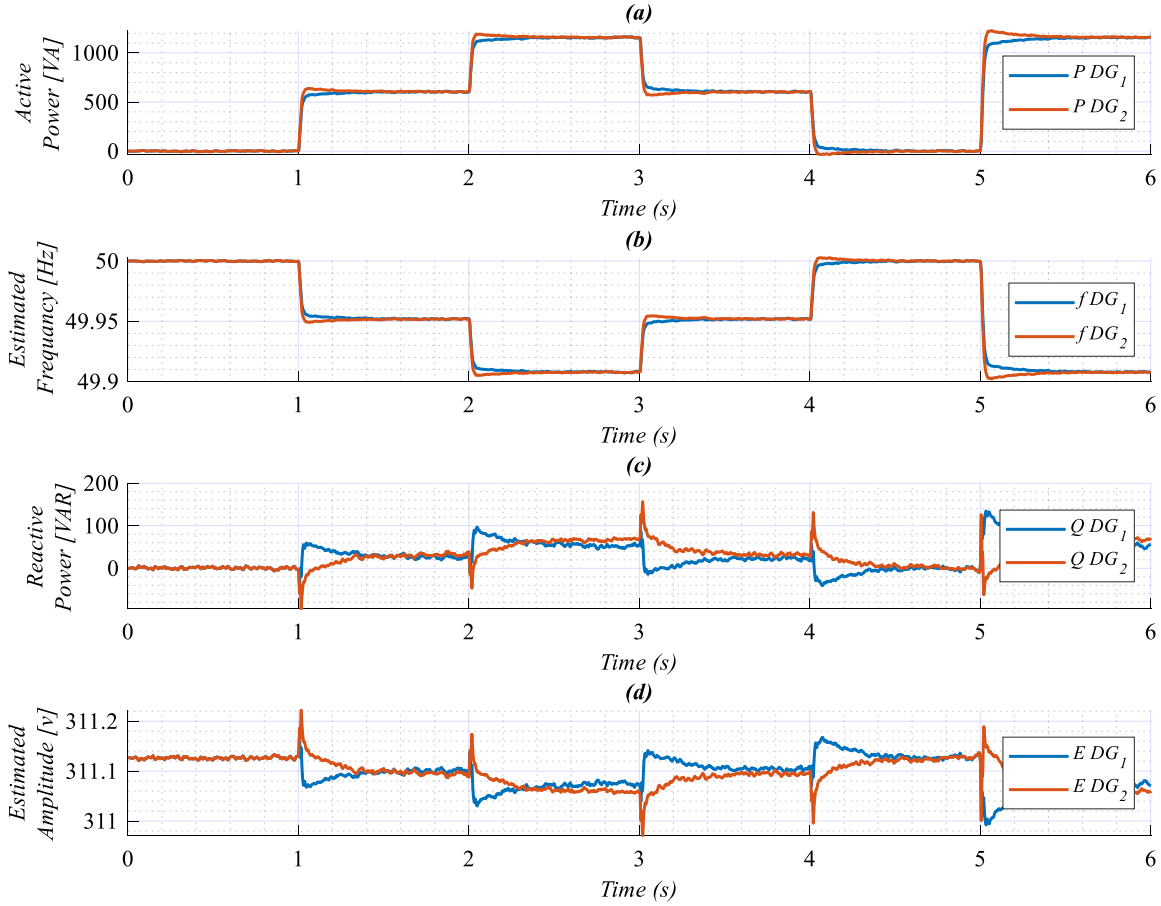


Fig. 4.17. *Time evolution of;* ***(a)*** *active powers,* ***(b)*** *output voltage frequencies,* ***(c)*** *reactive powers, and* ***(d)*** *output voltage amplitudes, of the of inverter 1 and 2 in response linear load change.*

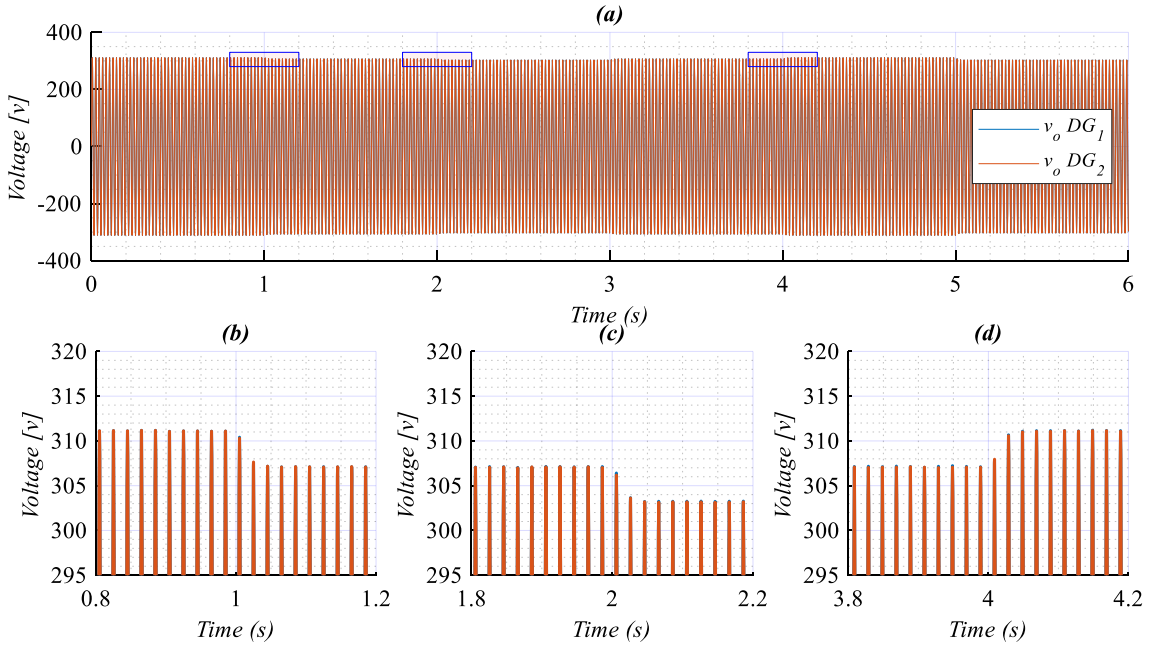
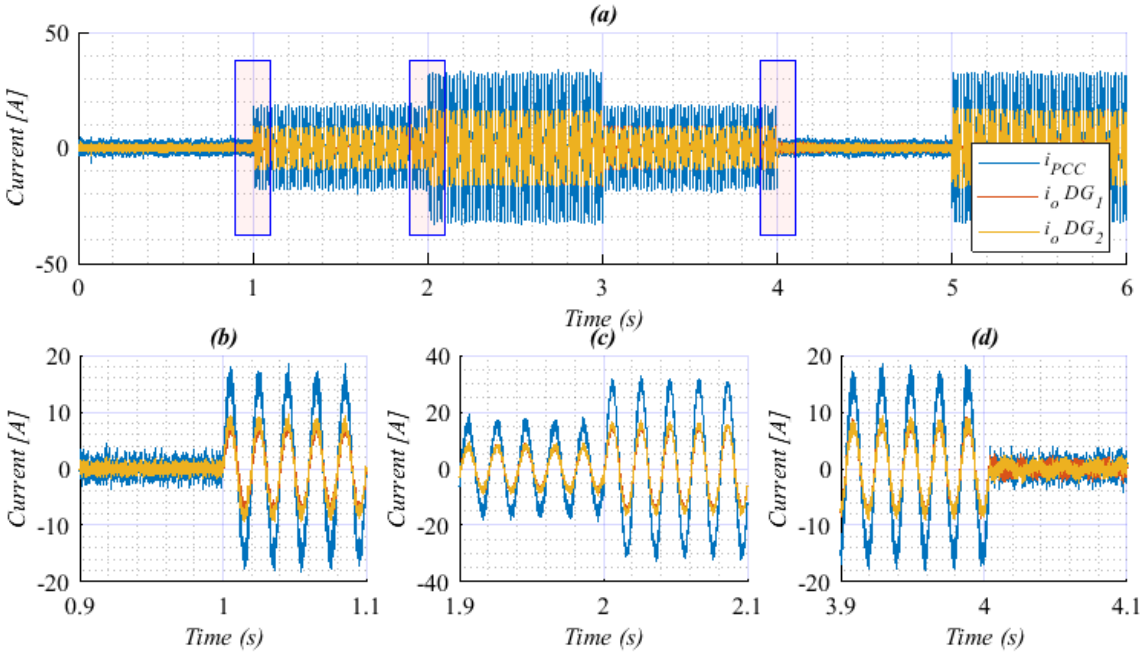


Fig. 4.18. *Time evolution of the inverters output voltages, and, zooms, in response linear load change.*



Figs. 4.19. *Time evolution of the inverters output currents, and, zooms, in response linear load change.*

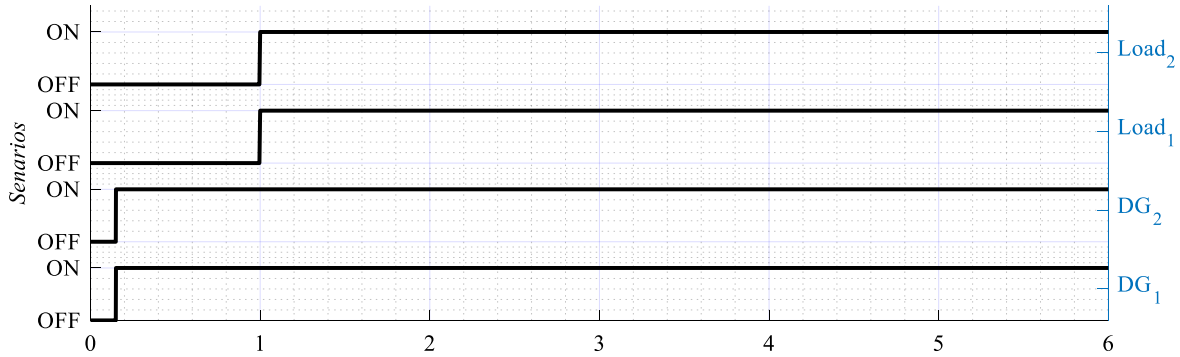
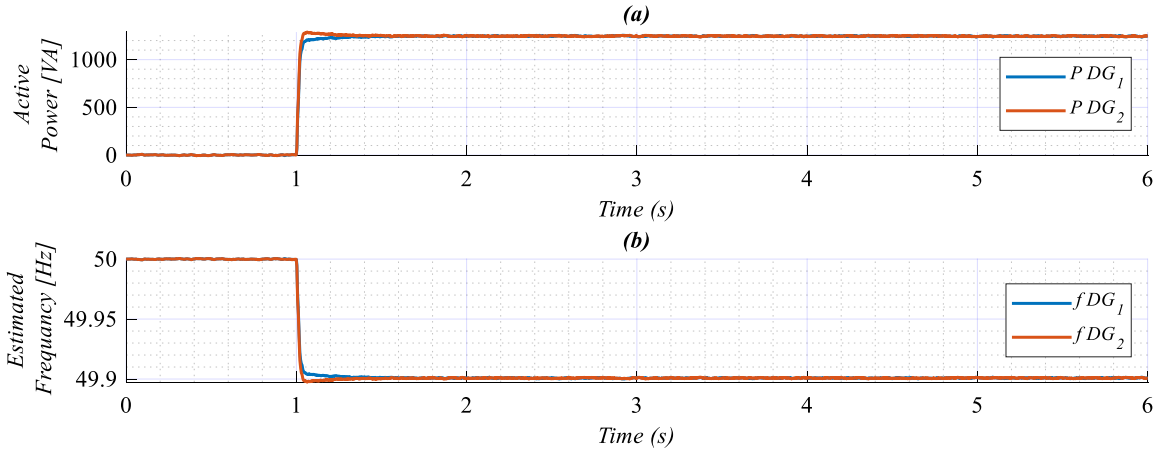


Fig. 4.20*. Plots of the performed scenarios for test 2.*



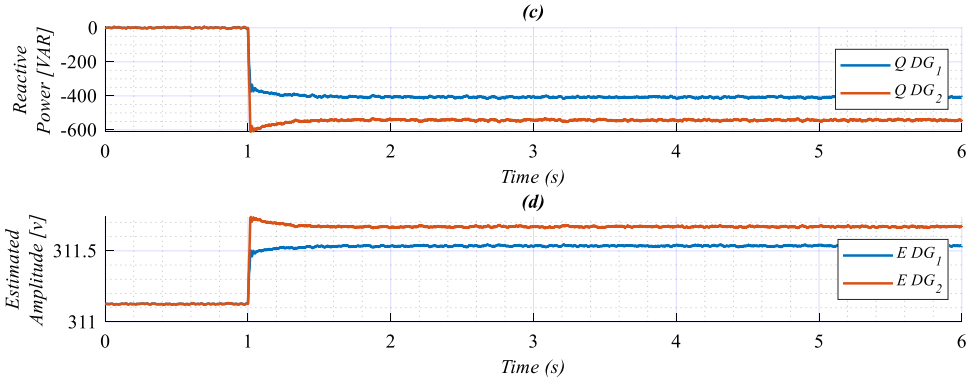


Fig. 4.21. *Time evolution of; (a) active powers, (b) output voltage frequencies, (c) reactive powers, and (d) output voltage amplitudes, of the of inverter 1 and 2 in response nonlinear load.*

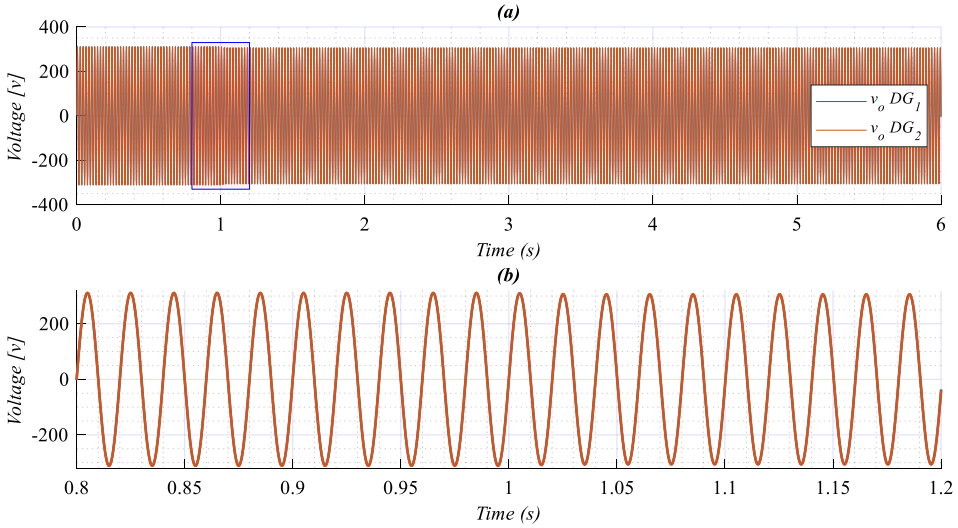


Fig. 4.22*. The performance of the proposed power control in front of sharing nonlinear load, VSIs output voltages, and zooms.*

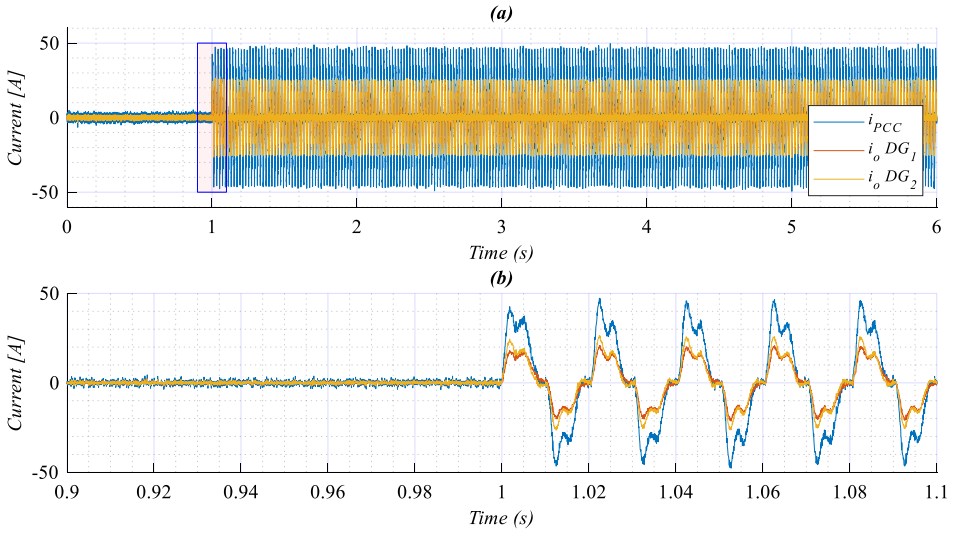


Fig. 4.23. *The performance of the proposed power control in front of sharing nonlinear load, VSIs output currents, and zooms.*

4.8 Experimental results

In order to validate the effectiveness of the proposed power-sharing control, an experimental setup of an islanded microgrid is conducted, as shown in **Fig. 4.24**. In this system, the ARM cortex microcontroller (STM32F407VGT6) is chosen as the main control chip with a switching frequency of 10 kHz for implementing the control strategy. Where each VSI's local controller is implemented in a separate microcontroller and without any communication between them. The main parameters taken in the tests are listed in the ***Table 4.4***. The same tests and scenarios as simulation cases are considered but at different times.

The obtained results during transient linear load are given in **Fig. 4.25, Fig. 4.26** and **Fig. 4.27** which depict the transient response of the active and reactive powers, frequencies, amplitudes, output voltages, and currents of the inverters and the load (at the PCC). According to these figures, one can be seen that at no load the power components and currents are zero, while f_{DG1}, f_{DG2}, $E_{DG1,}$ and E_{DG2} are set to the nominal values. When the loads are added and removed, it can be noticed that active and reactive powers are perfectly sharing between the inverters, showing good transient responses in terms of settling time and no overshoots as well as no ripples at steady state. Also, the f_{DG1}, f_{DG2}, $E_{DG1,}$ and E_{DG2} droop and grow with the same amounts, respectively, during the load transient to deliver the required load power. Further, they ensuring the pure sinusoidal form of the output voltage and current in this case.

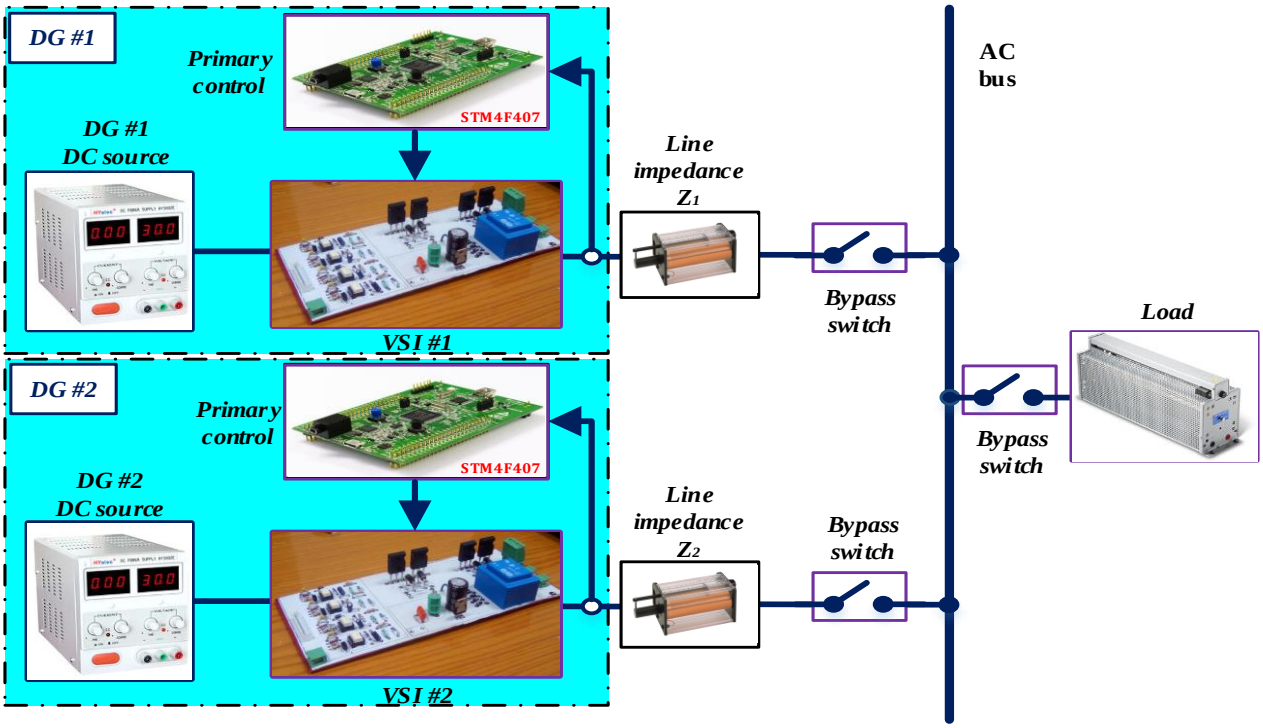


Fig. 4.24. The experimental setup of two parallel-connected VSIs.

Fig. 4.28 and **Fig. 4.29** highlight the results obtained in the case of sharing a nonlinear load, and they show the same variables as the first test. In these figures, one can be noted that when the nonlinear load occurs at t = 0.75 s, the inverters share accurately the active power delivered to the nonlinear load. In addition, f_{DG1} and f_{DG2} are dropped with equaled amounts according to the load demand, the same effect occurs for the reactive powers and amplitudes of the VSIs. Further, the output voltages and currents of the VSIs are matched, in which the currents have the same distorted forms as the load current form. Moreover, generally speaking, the presented figures demonstrate that all obtained variables have good transient responses and steady-state performances.

Table 4.4. VSIs Power Stages and Primary Control Level Parameters

Parameters	Symbol	Unit	Value
Nominal Voltage	E_n	V	24
Nominal frequency	f_n	Hz	50
Switching frequency	f_s	kHz	10
DC voltage	U_{DC}	V	32
Output filter capacitor	C	µF	26
Output filter inductor	L	mH	2.7
Line impedance of DG #1	L_1	mH	0.5
Line impedance of DG #2	L_2	mH	0.8
Virtual inductance	L_v	mH	4
Virtual Resistance	R_v	Ω	1
P-ω droop	m	-	0.0003
Q-*V* droop	n	-	0.003
Voltage controller P gain	k_{pv}	-	0.1307
Voltage controller I gain	k_{pi}	-	32.5476
Current controller P gain	k_{iv}	-	146×10^5

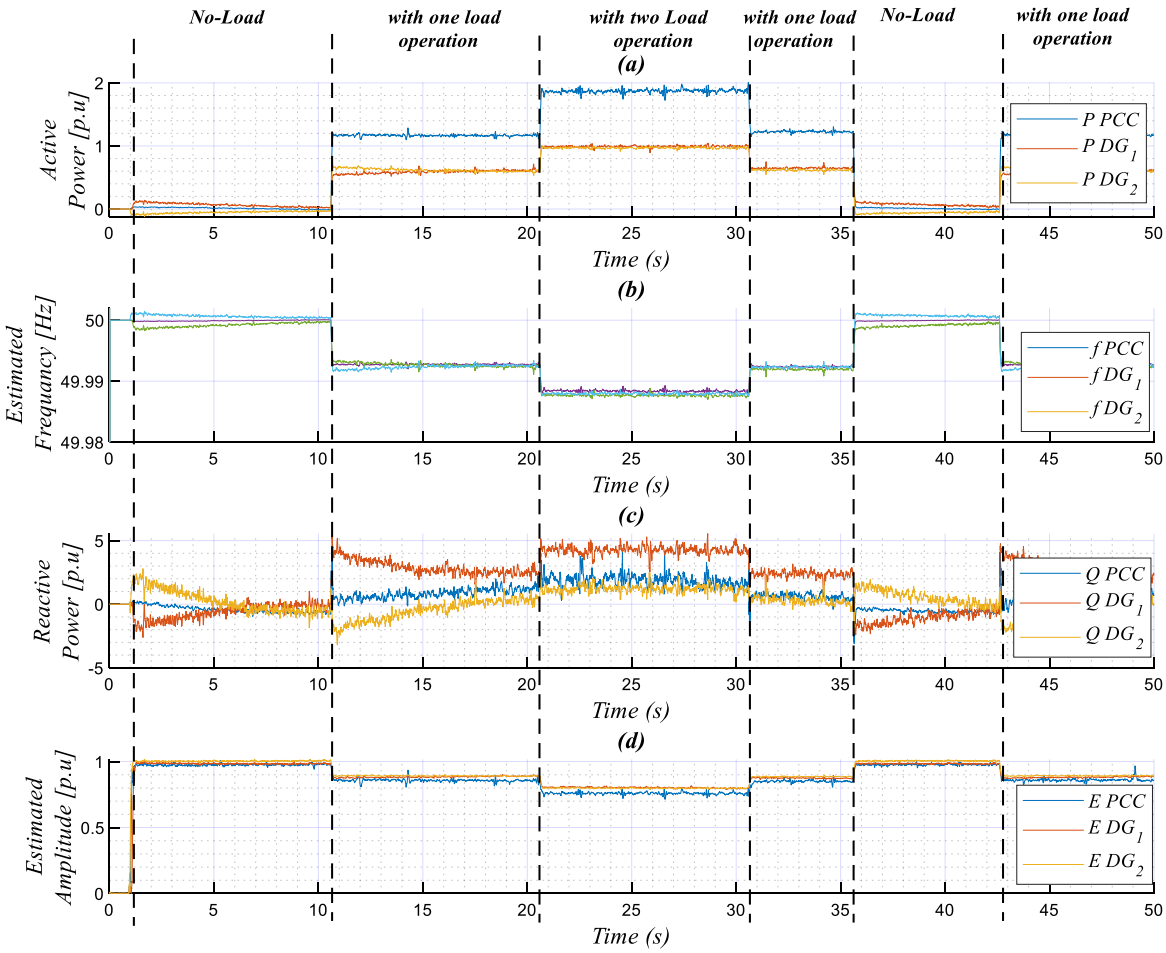


Fig. 4.25. *Transient responses of the inverters and the load;* ***(a)*** *active powers,* ***(b)*** *frequencies,* ***(c)*** *reactive powers, and* ***(d)*** *amplitudes in response to linear load change.*

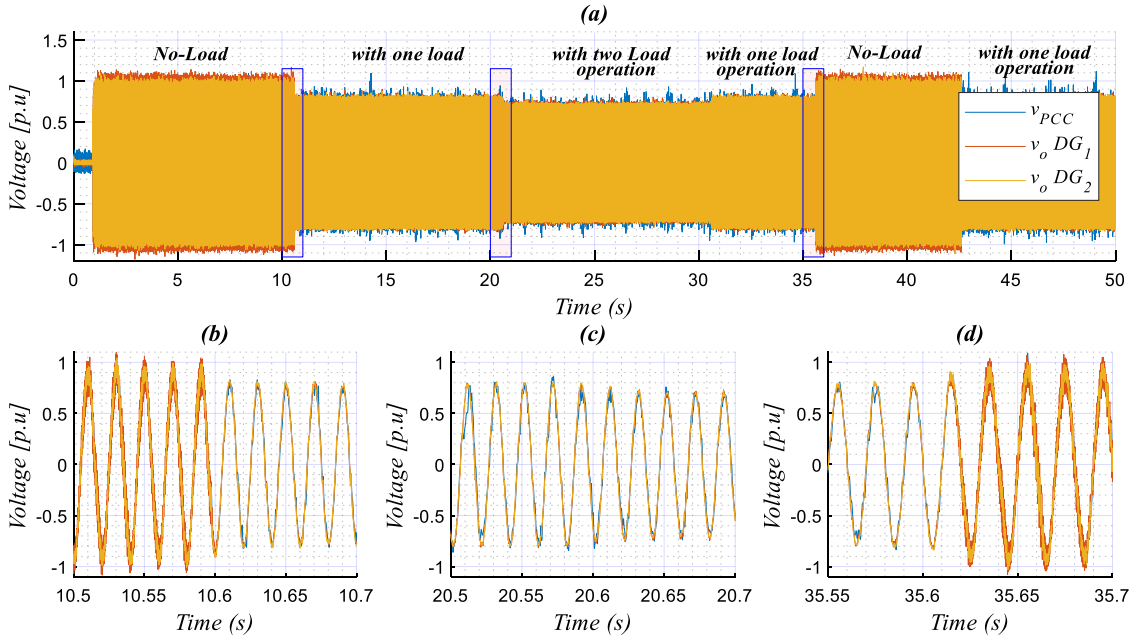


Fig. 4.26*.Transient responses of the output voltages, and zooms of the VSIs and the load, in the case of linear load change.*

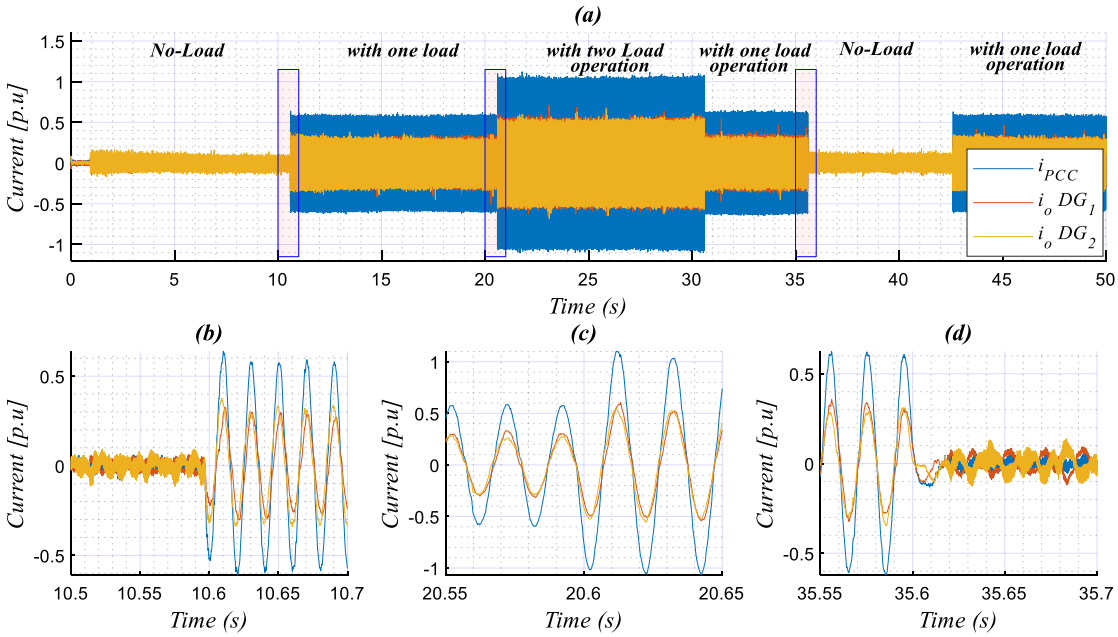


Fig. 4.27. *Transient responses of the output currents, and zooms of the VSIs and the load, in the case of linear load change.*

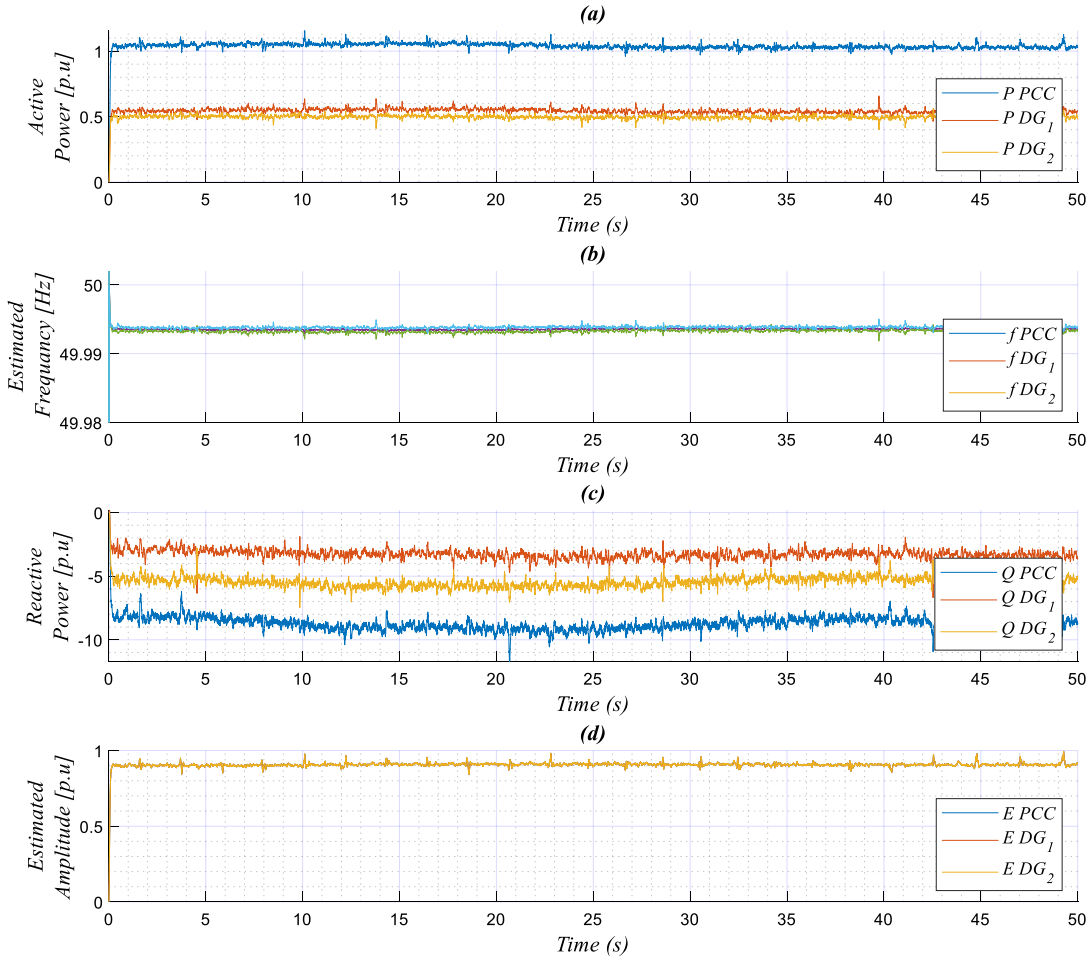


Fig. 4.28. *Transient responses of the inverters and of the load;* ***(a)*** *active powers,* ***(b)*** *frequencies,* ***(c)*** *reactive powers, and* ***(d)*** *amplitudes, for the case of supplying nonlinear load.*

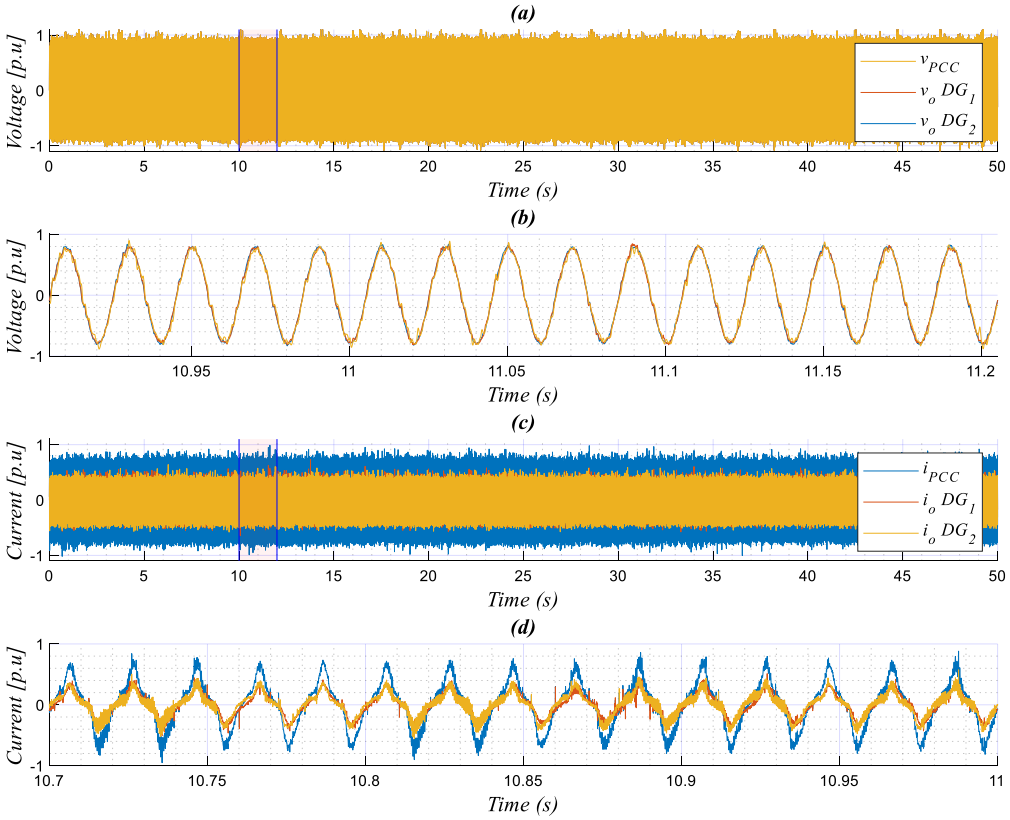


Fig. 4.29. *Transient responses of the output voltage and currents of the VSI and the at the PCC, and zooms, for the case of supplying nonlinear load.*

4.9 Conclusion

An improved droop-based control strategy, for achieving accurate power-sharing among single-phase parallelized VSIs considering linear and nonlinear loads, was proposed in this chapter. The proposed scheme involves a MESOGI-FLL based-enhanced power calculation method and frequency-adaptive virtual-impedance control loop. Computing the averaged powers using multiple ESOGI strategy-based power calculator was established. The use of MESOGI-FLL makes the power calculation, frequency-adaptive and DC component- and harmonic-immune, which lead to accurate P/Q calculation with fast transient response and low computational cost. In addition, as the model of the MSOGI has not been derived yet, MESOGI modelling and analysis are developed. The proposed method makes obtaining a fair condition of comparison with some reported power calculation methods. A performance comparison between the proposed method and these power calculation methods under normal and distorted operating conditions was then conducted. The simulation findings confirm that the proposed method offers proper power calculation with high rejection capability for DC component and current distortions and good trade-off relationship between harmonic rejection and transient response speed.

Furthermore, the design a frequency-adaptive virtual-impedance scheme based on the MESOGI-FLL strategy was adopted. This concept exploits the feature of the MESOGI-FLL regarding current components estimation to ensure accurate computation of the virtual-impedance voltage. Hence, this feature has contributed to improving the droop control performance in terms of current harmonics share among VSIs, especially when supplying nonlinear loads.

The performance of the proposed whole control scheme was evaluated both simulations and experiments to demonstrate its effectiveness for ensuring accurate power-sharing even in front of the DC component and nonlinear load distortion conditions. The obtained simulation results were proved that the proposal is effective for improving the active and reactive power sharing accuracy and enhance the system dynamical response. The presented experimental results were agreed with the simulation ones and validate the overall performance of the proposed control scheme.

Conclusions

Conclusions

In this thesis, some contributions to analyzing, modeling and designing enhanced control schemes involved into the primary control level intended for single-phase islanded MG were made.

- In chapter 1, an overview of the microgrid concept, architectures, and different operating modes was explained. In addition, the control of microgrid considering centralized and centralized approaches, and the hierarchy including primary, secondary and tertiary control levels was provided. A review on the research works related to the involved units into the primary control layer, i.e., droop control loop, virtual impedance and, inner control loop. The thesis objectives, main contributions and organization were presented.
- In chapter 2, an enhanced estimation scheme based on SOGI-FLL strategy, named ESOGI-FLL, suitable for DC offset rejection in single-phase system was proposed. An overview on the SOGI-FLL scheme and study on the effects of the DC offset in the output of the SOGI-FLL were presented. It was illustrated that the presence of a dc component in the SOGI-FLL input signal causes errors in the SOGI-FLL outputs, the quadrature component and the operating frequency. The schematic of the proposed ESOGI-FLL scheme, which based on adding DC rejection/estimation loop to the standard SOGI-FLL structure, was provided. Mathematical analysis investigates the ability of the proposed solution on rejecting the DC component effect in the outputs was developed. It was demonstrated that this solution solves both oscillatory and offset errors of the standard SOGI-FLL and makes it immune to disturbance effects of the dc component. Comparative study among the proposed scheme and the standard SOGI-FLL and TOGI-FLL schemes in term of the needed number of numerical operations for digital implementation of each scheme in a μC was investigated. Comparative simulation and experimental tests were conducted, demonstrating the performance of the proposed scheme in achieving accurate estimation of the expected parameters under various disturbances.
- Designing a scheme of the inner voltage and current control loops for single-phase VSIs was presented in chapter 3. This scheme is based on a PI with feedforward control strategy for regulating the VSI output voltage and a P controller for controlling the inductor current. voltage. The modeling of these control loops was presented, also, stability analysis and control design guidelines for tuning their control parameters were provided. The discretization aspect of the voltage and current control loops was given. The designed control scheme was applied to a single-phase LC-filtered VSI with a load. The Simulation and experimental results demonstrated that the proposed controller ensures current tracking with good transient

response and with zero error at steady state under different operating conditions.

- In chapter 4, enhanced power sharing control scheme for single-phase paralleled VSIs during islanded mode was designed. This scheme includes an improved power calculation scheme and robust virtual impedance control loop based on Multiple enhanced SOGI-FLL (MESOGI-FLL). An overview of the conventional, advanced, and recent methods for power calculation in single-phase application was presented. The model of the MSOGI-FLL, which cannot be found in the literature, was derived. Performance comparison study of the proposed scheme with other method regarding power calculation was conducted. It was demonstrated that this proposed method guarantees accurate power calculation with fast transient response compared to the stated methods. The schematic of the MSOGI-FLL based-robust virtual impedance loop was described. Stability analysis to system parameters, which allows effective selection of the virtual impedance parameters was presented. Simulation and experimental tests for two parallel-connected single-phase VSIs were conducted to verify the effectiveness of the proposed power sharing controller. The results were demonstrated that the proposed controller provides an accurate power sharing with fast transient behavior and high harmonic rejection ability even under highly distorted nonlinear load current.

Appendices

Appendix A: Expressions of the closed loop transfer function of the MESOGI-FLL

In this appendix the transfer functions, $G_{BF.\alpha-1,3,5,7}$, $G_{BF.\beta-1,3,5,7}$ and $G_{BF.DC}$, related the output components of the MESOGI-FLL to the input current. These transfer functions are given as follows:

$G_{BF.\alpha-1}$:
Num = [k*ω_o 0 83*k* ω_o^3 0 1891*k*ω_o^5 0 11025*k*ω_o^7 0];
Dem = [1 4*k*ω_o 84*ω_o^2 252*k*ω_o^3 1974*ω_o^4 3948*k*ω_o^5 12916*ω_o^6 … 12916*k*ω_o^7 11025*ω_o^8];

$G_{BF.\beta-1}$:
Num = [-k*ω_f (k*ω_o^2 - 3*$k^{2*}\omega_o$*ω_f) -83* k*$\omega_o^{2*}\omega_f$ (83*k*ω_o^4 - 169*$k^{2*}\omega_o^{3*}\omega_f$) ..
-1891* k*ω_o^4* k*ω_f (1891*k*ω_o^6 - 2057*$k^{2*}\omega_o^{5*}\omega_f$) - 11025*$k$*$\omega_o^{6*}\omega_f$ ...
(11025*k*ω_o^8 - 1891*$k^{2*}\omega_o^{7*}\omega_f$) 0];
Dem = [1 (ω_f + 4* k*ω_o) (84*ω_o^2 + 4* k*ω_o *ω_f) (252* k*ω_o^3 + 84*ω_f *ω_o^2)...
(1974*ω_o^4 + 252* k*ω_f*ω_o^3) (3948*k*ω_o^5 + 1974*ω_f*ω_o^4)...
(12916* ω_o^6 + 3948* k*ω_f *ω_o^5) (12916*k*ω_o^7 + 12916*ω_f *ω_o^6)...
(11025* ω_o^8 + 12916* k*ω_f *ω_o^7) 11025* $\omega_o^{8*}\omega_f$];

$G_{BF.\alpha-3}$:
Num = [k*ω_o 0 75* k*ω_o^3 0 1299* k*ω_o ^5 0 1225* k*ω_o^7 0];
Dem = [1 4*k*ω_o 84*ω_o^2 252*k*ω_o^3 1974*ω_o^4 3948*k*ω_o^5 12916*ω_o^6 …
12916*k*ω_o^7 11025*ω_o^8];

$G_{BF.\beta-3}$:
Num = [-k*ω_f (9* k*ω_o^2 - 3* $k^{2*}\omega_o$*ω_f) - 75* k*$\omega_o^{2*}\omega_f$ (675* k*ω_o^4 - 169*k^2*...
$\omega_o^{3*}\omega_f$) -1299*k*$\omega_o^{4*}\omega_f$ (11691*k*ω_o^6 - 2057*$k^{2*}\omega_o^{5*}\omega_f$) - 1225* k*$\omega_o^{6*}\omega_f$ ...
(11025*k*ω_o^8 - 1891*$k^{2*}\omega_o^{7*}\omega_f$) 0];
Dem = [3 (3*ω_f + 12* k*ω_o) (252*ω_o^2 + 12*k*ω_o*ω_f) (756* k*ω_o^3 + 252*ω_f*ω_o^2)...
(5922*ω_o^4 + 756*ω_f *k*ω_o^3) (11844* k*ω_o^5 + 5922*k*ω_f*ω_o^4) ...
(38748*w^6 + 11844*k*wf*w^5) (38748*k*w^7 + 38748*wf*w^6)...
(33075*ω_o^8 + 38748*k*ω_f*ω_o^7) 33075*$\omega_o^{8*}\omega_f$];

$G_{BF.\alpha-5}$:
Num = [k*ω_o 0 59* k*ω_o^3 0 499* k*ω_o^5 0 441*k*ω_o^7 0];
Dem = [1 4* k*ω_o 84*ω_o^2 252*k*ω_o^3 1974*ω_o^4 3948* k*ω_o^5 12916*ω_o^6 …
12916* k*ω_o^7 11025*ω_o^8];

$G_{BF.\beta-5}$:
Num = [-k*ω_f (25* k*ω_o^2 - 3*$k^{2*}\omega_o$*ω_f) - 59* k*$\omega_o^{2*}\omega_f$ (1475* k*ω_o^4…
+169*$k^{2*}\omega_o^{3*}\omega_f$) - 499*$k$*$\omega_o^{4*}\omega_f$ (12475* k*ω_o^6 - 2057*k^2* k*$\omega_o^{5*}\omega_f$) … -
441*k*$\omega_o^{6*}\omega_f$ (11025* k*ω_o^8 - 1891*$k^{2*}\omega_o^{7*}\omega_f$) 0];

Dem = [5 (5*ω_f + 20*k*ω_o) (420*ω_o^2 + 20*k*ω_o*ω_f) (1260*k*ω_o^3 + 420*ω_f *ω_o^2) … (9870*ω_o^4 + 1260*ω_f * k*ω_o^3) (19740* k*ω_o^5 + 9870*ω_f*ω_o^4) (64580*ω_o^6 + … 19740*ω_f*k*ω_o^5) (64580*k*ω_o^7 + 64580*ω_f* ω_o^6) (55125*ω_o^8 + 64580*ω_f*k*ω_o^7) … 55125*$\omega_o^{8*}\omega_f$];

$G_{BF.\alpha-7}$:

Num = [k*ω_o 0 35* k*ω_o^3 0 259* k*ω_o^5 0 225* k*ω_o^7 0];

Dem = [1 4* k*ω_o 84*ω_o^2 252*k*ω_o^3 1974*ω_o^4 3948* k*ω_o^5 12916*ω_o^6 … 12916* k*ω_o^7 11025*ω_o^8];

$G_{BF.\beta-7}$:

Num = [-k*ω_f (49*k*ω_o^2 - 3*$k^{2*}\omega_o$*ω_f) - 35*k*$\omega_o^{2*}\omega_f$ (1715*k*ω_o^4 -… 169*$k^{2*}\omega_o^{3*}\omega_f$) - 259*$k$*$\omega_o$^4* ω_f (12691*k*ω_o^6 - 2057* $k^{2*}\omega_o^{5*}\omega_f$) …. - 225*$k$*$\omega_o^{6*}\omega_f$ (11025*k*ω_o^8 - 1891*$k^{2*}\omega_o^{7*}\omega_f$) 0];

Dem = [7 (7*ω_f+ 28*k*ω_o) (588*ω_o^2 + 28*ω_f* k*ω_o) (1764*k*ω_o^3 + 588*ω_f*ω_o^2)...

(13818*ω_o^4 + 1764*ω_f* k*ω_o^3) (27636*k*ω_o^5 + 13818*ω_f*ω_o^4) ...

(90412*ω_o^6 + 27636*ω_f*k*ω_o^5) (90412*k*ω_o^7 + 90412*ω_f*ω_o^6)...

(77175*ω_o^8 + 90412*ω_f* k*ω_o^7) 77175*$\omega_o^{8*}\omega_f$];

$G_{BF.DC}$:

Num = [ω_f 0 84* ω_f *ω_o^2 0 1974* ω_f *ω_o^4 0 12916* ω_f * ω_o^6 11025*ω_f * ω_o^8]

Dem = [1 ω_f + 4* k*ω_o 84* ω_o^2 + 4*ω_f *k*ω_o 252* k*ω_o^3 + 84*ω_f *ω_o^2 … 1974*ω_o^4+252*ω_f *k*ω_o^3 3948*k*ω_o^5+1974*ω_f *ω_o^4 12916*ω_o^6+ 3948*k*ω_f*ω_o^5 … 12916*k*ω_o^7 + 12916*ω_f*ω_o^6 11025*ω_o^8 + 12916*ω_f*k*ω_o^7 11025*$\omega_o^{8*}\omega_f$].

The algorithm that determines the expressions of these transfer functions in MATLAB is given below.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                                    Script Matlab
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all
clc

syms  k...% SOGI-QSG gain
     wo...% Nominal frequency
     wf...% LPF cut-off frequency
      s...% Laplace operator

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% The closed loop transfer functions of the output components of the MESOGI-
QSG
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% a- The output components i_(α-n), which are in-phase with the input signal
%                          of each ESOGI-QSG block
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Ga_1 = k*wo*s/(s^2 + k*wo*s +    wo^2);
Ga_3 = k*wo*s/(s^2 + k*wo*s +  9*wo^2);
Ga_5 = k*wo*s/(s^2 + k*wo*s + 25*wo^2);
Ga_7 = k*wo*s/(s^2 + k*wo*s + 49*wo^2);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% b- The output components i_(β-n), which are, in quadrature-phase with
```

```
%                  the input signal of each ESOGI-QSG block
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Gb_1 = k*1*(wo^2)/(s^2 + k*wo*s +    wo^2);
Gb_3 = k*3*(wo^2)/(s^2 + k*wo*s +  9*wo^2);
Gb_5 = k*5*(wo^2)/(s^2 + k*wo*s + 25*wo^2);
Gb_7 = k*7*(wo^2)/(s^2 + k*wo*s + 49*wo^2);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% c- The transfer function of the dc-component (of the LPF)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  G_DC = wf/(s+wf);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% The closed-loop transfer functions of the output components
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
A = [  1,  Ga_1,  Ga_1,  Ga_1;...
    Ga_3,     1,  Ga_3,  Ga_3;...
    Ga_5,  Ga_5,     1,  Ga_5;...
    Ga_7,  Ga_7,  Ga_7,     1];

B = [Ga_1;Ga_3;Ga_5;Ga_7];

C = [   0,  Gb_1,  Gb_1,  Gb_1;...
     Gb_3,     0,  Gb_3,  Gb_3;...
     Gb_5,  Gb_5,     0,  Gb_5;...
     Gb_7,  Gb_7,  Gb_7,     0];

D = [Gb_1;Gb_3;Gb_5;Gb_7];
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Gs_Ma = collect(simplify((inv(A))*B),s);
Gs_Mb = collect(simplify(-C*(inv(A))*B+D),s);
Gs_MDC = collect(simplify((1-[1 1 1 1]*(inv(A))*B)*G_DC),s);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

Appendix B: Simulation models of the VSI with the primary control in MATLAB/Sim Power System environment

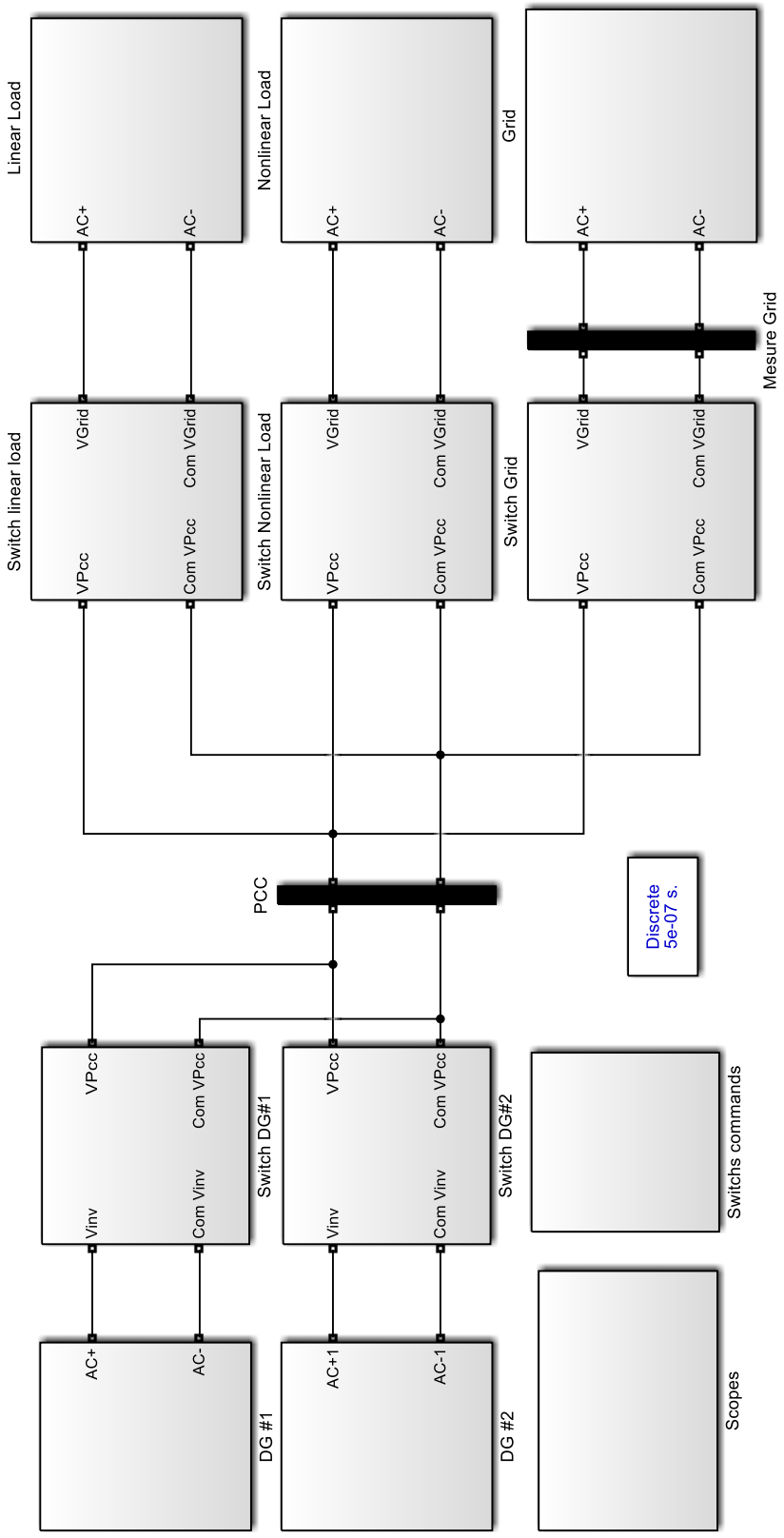


Fig. App.B.1. Simulation model of the DGs with their primary control supply linear and nonlinear loads.

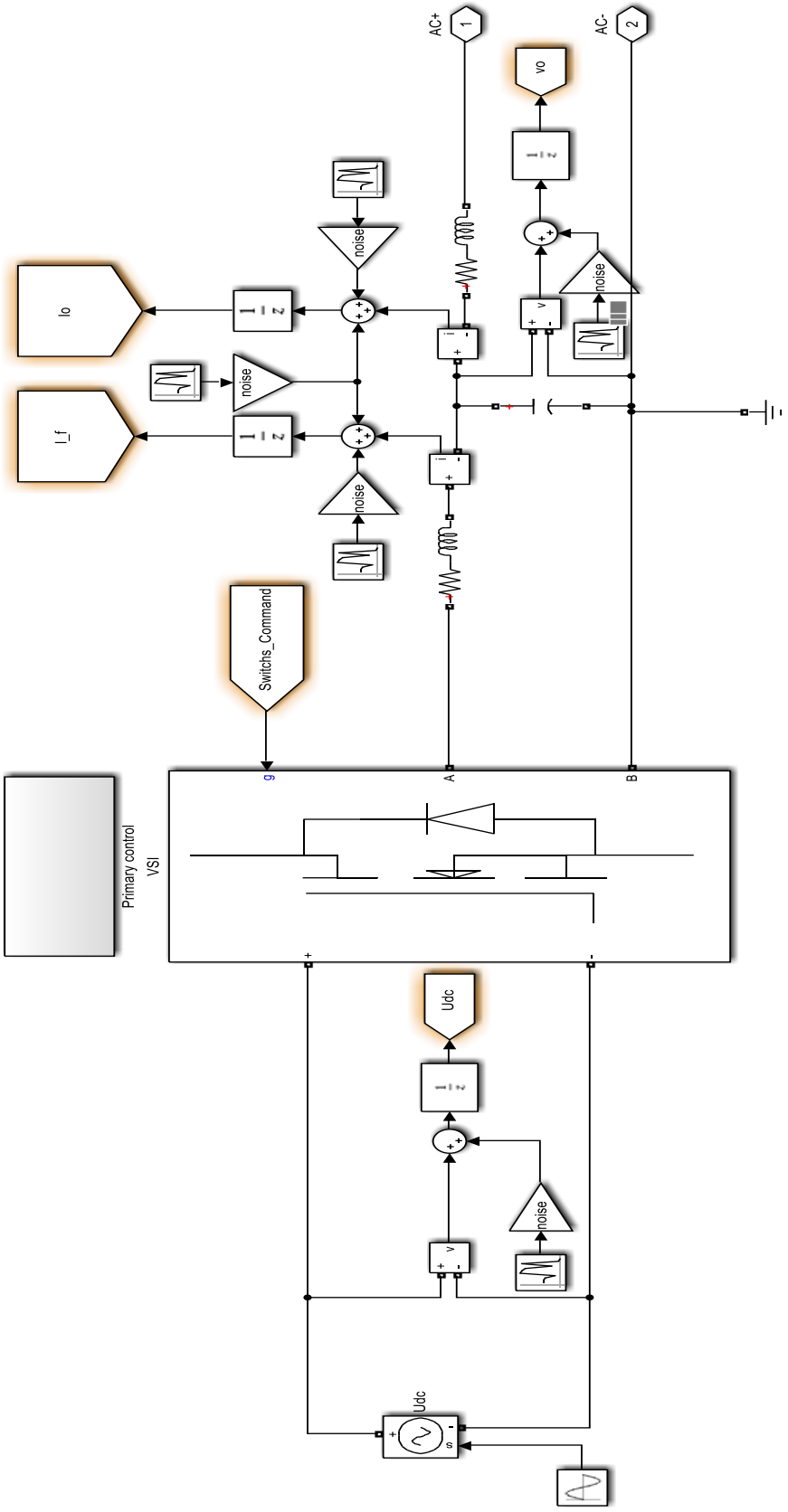
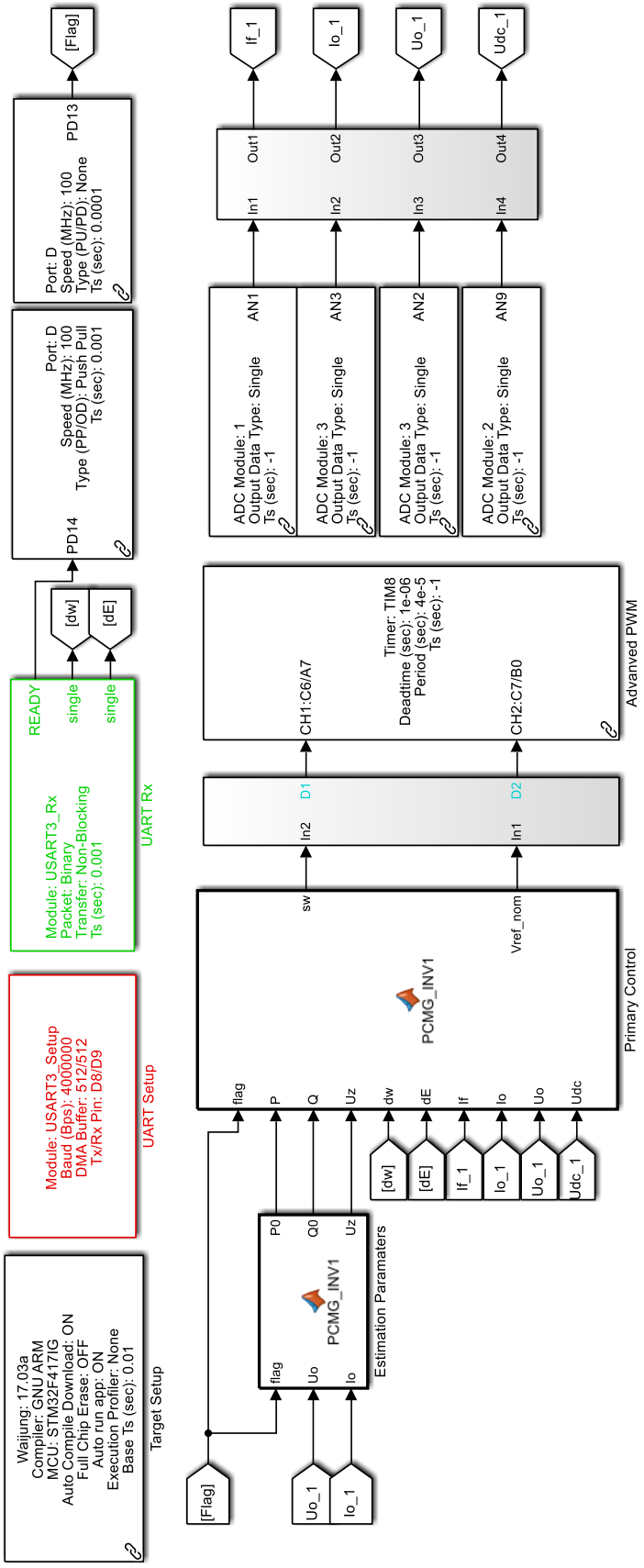


Fig. App.B.2. Simulation model of a VSI with the primary control.

Appendix C: Model of the implemented primary control in STM32F4 board based on MATLAB/Simulink



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