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Study of super junction diode performances using TCAD-SILVACO tools

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Acknowledgment

How enriching was this experience, which initially seemed like a simple routine activity. then, that it was our surprise when as and when the evolution of our work, we measured the gap which separated us from this mass of knowledge to fill to finish our memory thanks to god whom we could have courage, will and patience, and people who are totally committed to knowledge.

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ملخص: تم تصميم بعض مكونات الطاقة عالية الجهد باستخدام تأثير الوصلات الفائقة. هذا الأخير سوف يزيد بشكل كبير من انهيار الجهد ويقلل بشكل كبير من المقاومة في حالة المرور. في هذا العمل، سوف نقارن الصمام الثنائي البسيط مع الصمام الثنائي الخندق العميق والصمام الثنائي متعدد الوصلات من خلال تعديل بعض المعلمات التكنولوجية والهندسية للهياكل، وسيتم تقديم نتائج هذه الدراسة باستخدام محاكي لبرنامج سيلفاكو.

كلمات المفاتيح: عناصر الطاقة، متعدد الوصلات، انهيار الجهد، الصمام الثنائي.

Résumé : Certain composant de puissance à haute tension sont conçus en exploitant l'effet des super jonctions. Ce dernier permettra d'augmenter sensiblement la tension de claquage et réduit drastiquement la résistance à l'état passant (Ron). Dans ce travail, nous allons comparer une diode simple a jonction pn et une diode a tranchée profonde et une diode a super jonction en modifiant des certains paramètres technologiques et géométriques des structures, les résultats de cette étude seront présentés à l'aide du simulateur Atlas du logiciel Silvaco.

Mots clés : composant de puissance, super jonction, tension de claquage, diode.

Abstract: Some high voltage power components are designed utilizing the effect of super junctions. The latter will significantly increase the breakdown voltage and drastically reduces the resistance in the on state (Ron). In this work, we will compare a simple pn-junction diode with a deep trench diode and a super-junction diode by modifying some technological and geometrical parameters of the structures. The result of this study will be presented using the ATLAS simulator of Silvaco software.

Keywords: power components, super junction, breakdown voltage, diode.

Lists of acronyms and abbreviations

Si :	Silicon.
N_A :	Donnor concentration (cm^{-3}).
N_P:	Acceptor concentration (cm^{-3}).
q:	Elementary electric charge ($1.6*10^{-19}$ c).
μ_n :	Electron mobility (cm^2/Vs).
μ_p :	Holes mobility (cm^2/Vs).
T:	Temperature (K).
V:	Voltage (v).
ρ:	Resistivity (Ω-cm).
W:	Space charge width (cm).
ε_s:	Relative dielectric permittivity of the semiconductor (11.9)
ε_0:	Absolute permittivity of the vacuum ($8.85*10^{-12}$ F/cm).
P :	Hole concentration (cm^{-3}).
n :	Electron concentration (cm^{-3}).
BV :	Breakdown voltage (v).
J_n:	Current density of electrons(A/cm^2).
J_p:	Current density of holes (A/cm^2).
K:	Boltzmann constant ($1.38*10^{-23}$ jk^{-1}).
I:	Electric current (A).
Φ_0:	Internal potential (V).
Is:	Saturation current (A).
R:	Resistance (Ω).
Ec :	Conduction band .
Ev:	Valence band.

SJ: Super junction.

Wpp: Maximum depletion width (cm).

Ec: Critical electric field (V/cm).

Ron: ON state resistance (Ω).

W_N, W_P: Width (cm).

H: Height (cm).

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General introduction

Power electronics has therefor been evolving for several decades, indeed thanks to the arrival of power components and developments of renewal energies, the field of semiconductors power components is now expanding strongly. Power semiconductors devices are many terminal devices that controls the flow of energy throughout electronic systems and they are made of silicon, three main parameters define the application range for a power device: R_{ON}(ON-state resistance), BV (breakdown voltage), switching time from ON to the OFF state. The power semiconductor devices have a trade-off relationship between breakdown voltage and ON- resistance.

The revolution of super junction technology are new standards in the field of energy efficiency specially used in MOSFET transistors and its address applications such in smartphones and tablets: chargers, audio and tv: power supplies and in telecommunications: PC power. So, we find them in low and higher power. The super junction consists of an alternation of N and P doped regions allowing to no longer have a voltage resistance inversely proportional to the doping. And the realization of the super junction goes trough of many epitaxial steps.

In this thesis we are purposing a thorough understanding of the super junction structure and operation, and we are doing an investigation of performances of a super junction diode, this investigation will concern the evaluating of the breakdown voltage of the super junction using a simulation tool of Silvaco-TCAD software.

General introduction

This thesis is organized into three chapters:

Chapter 1: this chapter present the fundamental notions of semiconductors, the breakdown voltage of a pn junction reversed biased. And we are covering the super junction diode.

Chapter 2: in this chapter we are talking about simulation tool used in our study whose name is ATLAS of Silvaco- TCAD software and we are giving some examples in super junction diode.

Chapter 3: this chapter present the simulation steps and the obtained results of a super junction performances (breakdown voltage) and we are comparing it with a conventional diode.

Finally, we are finishing with a general conclusion and some perspectives.

Chapter1. Generality of Semiconductors

1.1 Introduction

Electronic devices such as diodes, transistors, and integrated circuits are made of a semi conductive material. To understand how these devices work, we should know the structure of atoms and the interaction of atomic particles.

Semiconductors are a solid element that can conduct electricity and they are coming between metals and insulators; the best-known semiconductors are Silicon (Si) but they are many other semiconductors besides (Si).

In this chapter we are talking about definitions of semiconductors and we used a reversed biased p-n junction specially the breakdown voltage and finally we have the new technology called super junction and will be comparing them with conventional diode (p-n junction).

1.2 semiconductors

1.2.1 Definition of semiconductors

All materials are made up of atoms; these atoms contribute to the electrical properties of a material, including its ability to conduct electrical current. Any material that will support a generous flow of charge when a voltage source of limited magnitude is applied (e.g. Copper (Cu); Silver (Ag); Gold (Au)) is conductor. The material that offers a very low level of conductivity under pressure from an applied voltage source (e.g. Mica, Quartz, Plastics, Glass) is called insulator. Whereas, semiconductor is a material that has a conductivity level somewhere between the extremes of an insulator and a conductor, and can be a pure element such as Germanium (Ge); or Silicon (Si); Boron (B), or they can be compounds such as cadmium selenide or gallium arsenide.

Inversely related to the conductivity of a material is its resistance to the flow of charge or current as given by: $R=\rho L/s$, where ρ = resistivity = $\Omega.cm$. For Copper (Cu): ρ=10 $^{-6}\Omega cm$, Si (Silicon): ρ=50×103Ωcm and Mica: ρ=10 $^{16}\Omega cm$. **[1]**

1.2.2 semiconductors types

Intrinsic semi-conductor: the resistivity of pure silicon is of the order of $\rho=10^{3}\Omega.cm$.

Extrinsic semiconductor: the resistivity of doped silicon with Bore or Phosphor is of the order of $\rho=10^{-2}\Omega.cm$.

1.2.3 Energy bands in semiconductors

Due to the intermixing of atoms in solids, instead of single energy levels, there will be bands of energy levels formed. These set of energy levels, which are closely packed are called as **Energy bands**.

- **Valence band:** is the *band having the highest occupied energy*.
- **Conduction band:** is the *band having the lowest occupied energy*.
- **Forbidden energy gap**: it's the gap between valance band an conduction band.

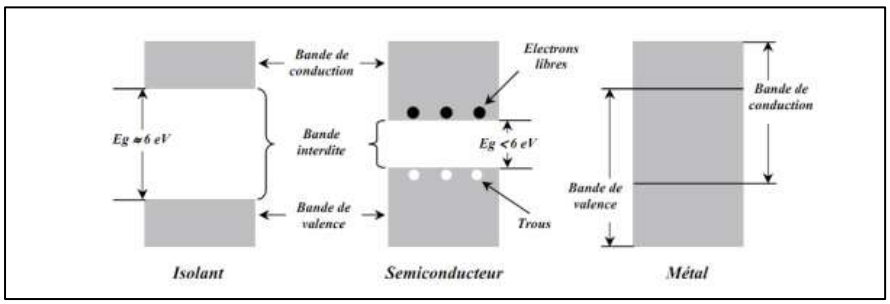


Figure 1.1 Structure in energy bands of materials.

1.3 P N junction

1.3.1 Definition

The *p-n* junction is the fundamental building block of the electronic age. Most electronic devices are made of silicon. By exploring the electrical properties of silicon, it is possible to acquire an understanding of the inner workings of the p-n junction.

A silicon crystal will have mobile electrons or holes depending upon the doping. As electrons and holes each have an electric charge, they are of course affected by electric fields. Another important effect is the random thermal motion of the electrons and holes. This type of motion is called diffusive flow and is important in understanding p-n junctions and solar cells. **[2]**

The p-n junction is a basic structure in the components. Since the components are formed of differently doped semiconductors, the p-n or np junctions are present at the interfaces. It is therefore essential to understand the physical phenomena that manifest themselves there. The p-n junction is also a component in itself. The function of this component is to let the current flow in one direction. It thus makes it possible to transform an alternating signal into a unipolar signal. This function is widely used in electronic power supply or radio frequency detection systems. (J, 2010)

1.3.2 Diffusion

This is a purely random phenomenon and is not related to any local concentration of perfume in the air: perfume atoms will drift randomly until eventually there is an even distribution of perfume molecules in the classroom's air.

In an n-type phosphorus doped silicon crystal the free electrons will diffuse, like perfume in a classroom, throughout the crystal in a purely random fashion until there is an equal distribution of free electrons throughout the volume of the n-type silicon crystal. In a p-type boron doped silicon crystal the corresponding holes will become equally distributed throughout the p type crystals volume.

The presence of a space charge causes the existence of an electric field and a potential variation. The potential varies from a value V_p in the p-type neutral region to a value V_n in the n-type neutral region. The difference between these two regions constitutes a potential barrier called diffusion voltage, due to the fact that it is the barrier that balances the diffusion forces.

$$V_D = V_N - V_P$$

The voltage V_d can be calculated in two ways by simply writing that the structure is in thermodynamic equilibrium. The first is to write that the level of Fermi is horizontal throughout the structure, the second is to write that the energy transfers are zero, that is to say that the currents of electrons and holes are zero.

Let's write that the Fermi level is the same throughout the structure. The electron densities in each of the regions are written Abrupt junction at thermodynamic equilibrium

$$N_n = N_c \exp\frac{(ECn - Ef)}{kt}$$

$$N_p = N_c \exp\frac{(ECp - Ef)}{kt}$$

which allows to write:

$$E_{cp} - E_{cn} = kt \ln \frac{Nn}{Np} = kt \ln \frac{Nd\ N\ a}{Ni^2}$$

The difference in energy E_{cp}-E_{cn} is the potential energy difference of the conduction electrons between the p-type region and the n-type region. Indeed, the electrons and the holes involved in the conduction being located at the ends of the bands, their kinetic energy is zero since the group velocity is zero (extremum of the energy function) and all their energy is potential.

$$V_d=V_n-V_p = \frac{(Ecp-Ecn)}{e}$$

The diffusion voltage is therefore given by the expression:

$$V_d = \frac{kt}{e} \ln \frac{Nd\, N\, a}{Ni^2}$$

For the doping used in practice and taking into account the values of ni at ambient temperature, the values of Vd are respectively of the order of 0.7 V and 0.35 V in the silicon and germanium junctions.

Now let's write that the current of each type of carrier is zero

$$J_n = \mu_n \{en\, E + KT(\frac{dn}{dx}) \}=0$$

$$J_p = \mu_p \{ep\, E - KT(\frac{dp}{dx}) \}=0$$

Which makes it possible to write the differential equations

$$\frac{dn}{n}= \frac{-e}{kt} E\, dx =\frac{e}{kt}\, dv$$

$$\frac{dp}{p}= \frac{e}{kt} E\, dx =\frac{-e}{kt}\, dv$$

By integrating the equation throughout the space charge area, ie we get

$$ln \frac{n(Xn)}{n(Xp)}= \frac{e}{kt} (v_n-v_p) =\frac{e}{kt} V_d$$

By explaining carrier densities of porters $n(x_n)=Nd$ et $n(x_p)= ni^2/Na$, we obtain for the diffusion voltage Vd the same expression as before

1.3.3 Formation of p-n junction

Doping one side of a piece of silicon with boron (a p-type dopant) and the other side with phosphorus (an n-type dopant) forms a *p-n* junction. First, however, consider two separate pieces of silicon - one being n-type, the other being p-type (see Figure 1.2).

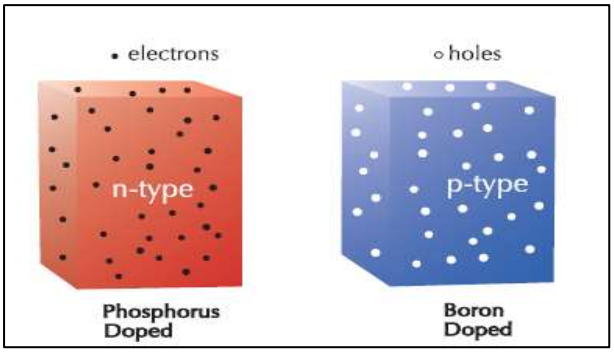


Figure1.2 Doped silicon.

The n-type material has large numbers of free electrons (negatively charged) that can move through the material. The number of positively charged phosphorus atoms (called positive ions), which are not free to move, exactly balance the number and charge of these negative free electrons. Similarly, for the p-type material, there are large numbers of free holes (positively charged) that can move through the material. Their number and positive charge is exactly counter-balanced by the number of negatively charged boron atoms (called negative ions). Now imagine that the n-type and the p-type materials are brought together (see figure 1.3).

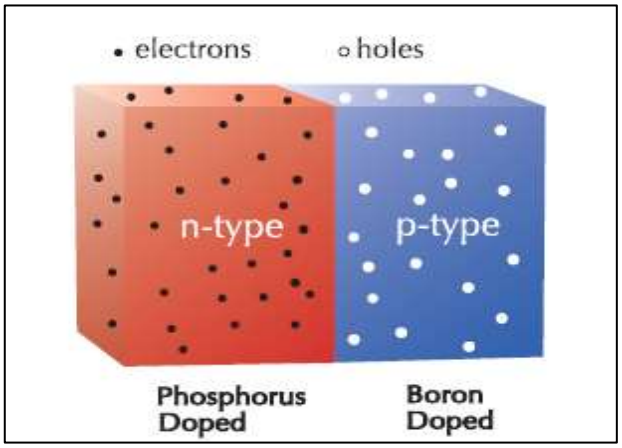


Figure 1.3 *n-type and p-type materials brought together.*

It is interesting to see what happens to the electrons and holes once these two pieces of silicon are joined. Due to the doping of the silicon crystal, there are large numbers of mobile electrons on the n-type side, but very few mobile electrons on the p-type side. Because of the random thermal motion of the free electrons, electrons from the n-type side start to diffuse into the p-type side. Similarly, due to the doping of the silicon, there are large numbers of mobile holes on the p-type side, but very few mobile holes on the n-type side. Holes in the p-type side, therefore, start to diffuse across into the n-type side.

Now, if the electrons and holes had no electric charge, this diffusion process would eventually result in the electrons and holes being uniformly distributed throughout the entire volume. They do, however, have an electric charge and this causes something interesting to happen! As the electrons in the n-type material diffuse across towards the p-type side, they leave behind positively charged phosphorus ions, near the interface between the n and p regions. Similarly, the positive holes in the p-type region diffuse towards the n-type side and leave behind negatively charged boron ions.

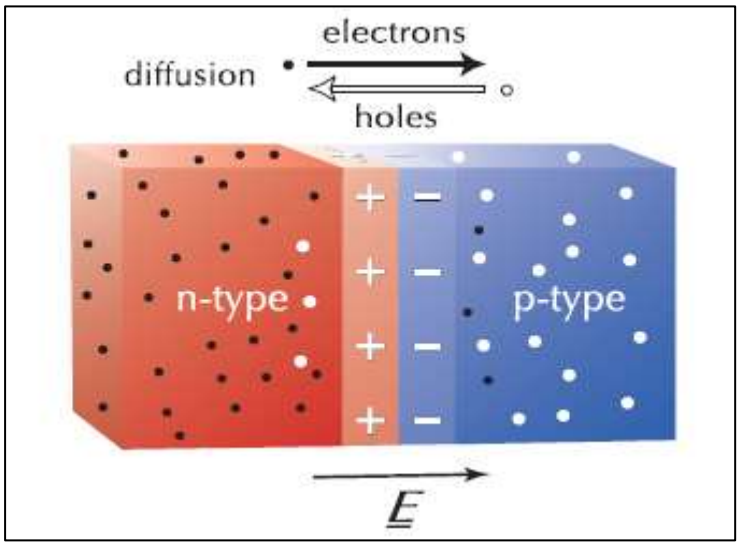


Figure1.4 *Diffusion establishes "built-in" electric field.*

These fixed ions set up an electric field right at the junction between the n-type and p-type material. This electric field points from the positively charged ions in

the n-type material to the negatively charged ions in the p-type material. The free electrons and holes are influenced by this "built-in" electric field with the electrons being attracted towards the positive phosphorus ions and the holes being attracted towards the negative boron ions.

Thus, the “built-in” electric field causes some of the electrons and holes to flow in the opposite direction to the flow caused by diffusion.

In a process called "diffusion", the random motions of mobile electrons and holes over time cause them to attempt to distribute equally within the total volume. As they cross the junction, the fixed ions they leave behind establish a "built-in" electric field.

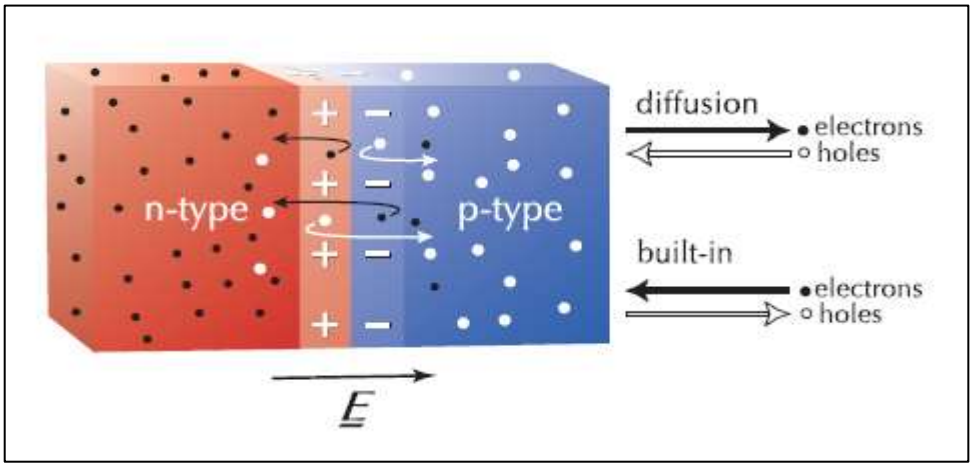


Figure1.5 Motion of mobile electrons and holes due to diffusion and the “built-in” electric field.

A mobile electron or hole near the "built-in" electric field will be attracted and swept back into its original volume. At the junction there are two effects occurring (1) diffusion with electrons moving from n-type to p-type and, (2) the "built in" electric field sweeping locally affected electrons back into the n-type volume. The

holes are affected similarly but in. These opposing flows eventually reach a stable equilibrium with the number of electrons flowing due to diffusion exactly balancing the number of electrons flowing back due to the electric field. The net flow of electrons across the junction is zero and the net flow of holes across the junction is also zero. This begs the question, "If there is no net current flowing, of what use is it?" Although there is no net flow of current across the junction there has been established an electric field at the junction and it is this electric field that is the basis of the operation of diodes, transistors and solar cells. **[2]**

1.3.4 Diode under biasing

- **No biasing condition (Vd=0V):** Minority carriers (say holes) in the n-side near the depletion region pass directly into the p-side (similarly minority electrons in the p-side pass directly into the n-side). The closer the minority carrier is to the junction, the greater the attraction for the layer of negative ions and the less opposition of the positive ions in the depletion region of the n-type material. The majority carriers (electrons) of the n-side must overcome the attractive forces of the layer of positive ions in the n-side and the shield of negative ions in the p-side to migrate into the area beyond the depletion region of the p-side. Only a few majority carriers with sufficient Kinetic Energy pass through the depletion region. In the absence of an applied bias voltage, the net flow of charge in any one direction for a diode is 0.

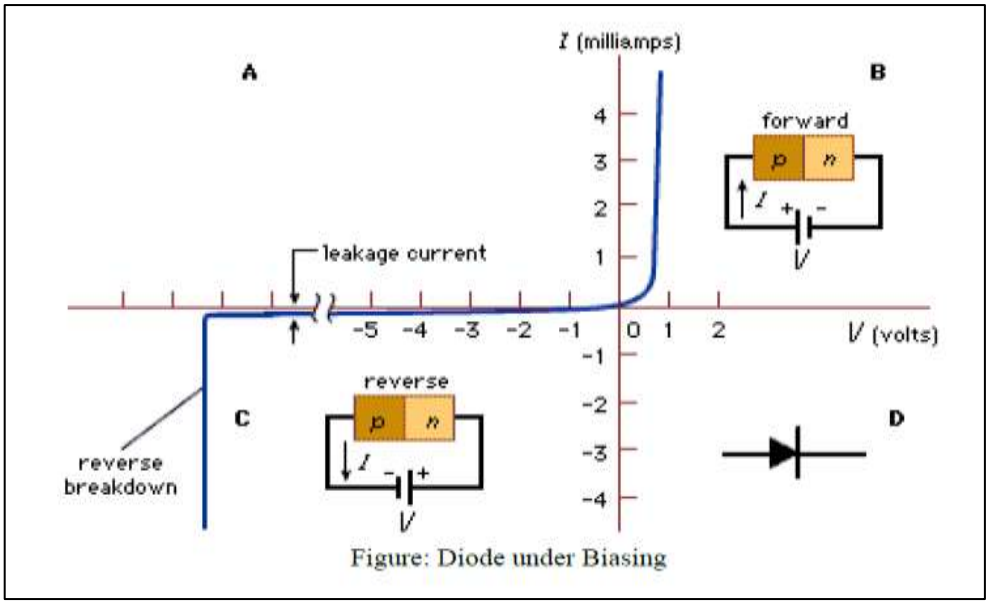


Figure1.6 diode under biasing.

- **Forward biasing condition (Vd>0V)**

Positive terminal of external potential is connected to n-side and the negative terminal to p-side. Large number of electrons in n-type material is drawn to the positive terminal and holes in p-type material is drawn to the negative terminal. As the forward voltage is increased to the knee of the characteristic, the barrier potential is progressively reduced to 0, allowing more and more majority charge carriers to flow across the junction. Beyond the knee of the characteristic, the potential barrier is completely eliminated, forward current increases almost linearly with the increase in forward voltage and the P-N junction starts behaving as a resistor. If the forward voltage is increased beyond a certain value, extremely large current will flow and the P-N junction may get destroyed due to overheating. Forward resistance of p-n junction is low (about 75 ohms in Ge and 150 ohms in Si).

- **Reverse biasing condition (Vd<0)**

When the reverse bias is applied, the potential barrier at the junction is increased. Therefore, the junction resistance becomes very high and there is no possibility of majority carriers flowing across a reverse biased junction. But still minority carriers generated on each side can cross the junction. This result in a very small current known as reverse saturation current. It is typically less than 1uA and may be also low as 1nA. Only very small reverse voltage is necessary to direct all minority carriers across the junction. On increasing the reverse voltage, a point may reach at which the junction breaks down with sudden rise in reverse current. This value of reverse voltage is called breakdown voltage (VBR). The maximum reverse voltage that can be applied to the P-N junction without any damage to the junction is known as Peak Inverse Voltage (PIV) and the maximum power that can be dissipated at the junction without any damage to it is called Maximum Power Rating (MPR).

1.3.5 space charge region (SCR)

After forming the junction between the two types of semiconductors, an internal potential of the junction ϕ0 appears between the two intrinsic Fermi levels EFi. The origin physics of this internal potential ϕ0 is the diffusion of the charge carriers. Indeed, the contacting of the semiconductors favors the diffusion of the electrons (e-) from the N-doped region to the P-doped region (low in electrons) and leave behind positive charges. Similarly, positive charges (holes h+) of the P-doped region diffuse to the N-doped (hole-poor) region and also leave behind negative charges. At the end of this process of disseminating load carriers, a permanent equilibrium is established and a poor area with free carriers is formed. This zone is called space charge zone or also "depletion zone". In order to study the electrostatic potential in the junction (space charge zone), the resolution of the Poisson equation is necessary. The Poisson equation is written:

$$\nabla^2 V(x, y, z) = div\ grad\ (V(x, y, z)) = -\rho \frac{(x,y,z)}{\varepsilon} \qquad (1)$$

With: $\nabla^2 V(x, y, z) = (d^2v/dx^2)+(d^2v/dy^2)+(d^2v/dz^2)$

The electric field E and the voltage V are connected by equation:

E=-grad V ⟹ $\text{div}(E)= \rho \frac{(x,y,z)}{\varepsilon}$

For a single dimension analysis (1 D),Poisson's equation becomes:

$$\frac{d^2v}{dx^2}=- \frac{\rho(x)}{\varepsilon}$$

With E=(-dv/dx)

$$\frac{d^2v}{dx^2}=- \frac{dE}{dx} =- \frac{\rho(x)}{\varepsilon}$$

With $\rho = q (p-n + N_D^+ - N_A^-)$ density volume of local charge.

$\varepsilon_0 = 8.854\times10^{-14}$ F/cm	Permittivity of the void
$\varepsilon_{rSi} = 11.7$	relative permittivity of silicon
$\varepsilon_{Si} = \varepsilon_{rSi} \times \varepsilon_0$	permittivity of silicon

In the space charge zone ($\rho\neq0$), the evolution of the potential has a curvature ($d^2v/dx^2\neq0$) and thus the revolution of the energy bands Ec(x), Ev(x) directly linked to that of the potential V(x). because: -**$qdV(x) = dEv(x)= dE_c(x)$.** **[4]**

1.3.6 fundamental equations

- Poisson equation:

$$\text{div } E = -\frac{\rho}{\varepsilon sc} \quad \text{with:} \quad E=-\text{grad}(V)$$

- Transport equation:

$$J_n = q\, n\, \mu_n\, E + q\, D_n\, \text{grad}\,(n)$$

$$j_p = q\, p\, \mu_p\, E - q\, D_p\, \text{grad}\,(p)$$

- Continuity equation:

$$\text{div}\, j_n = q\, \frac{\partial n}{\partial t} + q\, U_n$$

$$\text{div}\, j_p = q\, \frac{\partial p}{\partial t} - q\, Up$$

- Displacement current:

$$J_{dep} = \varepsilon_{sc}\, \frac{\partial E}{\partial t}$$

$$J_{total} = j_n + j_p + \varepsilon_{sc}\, \frac{\boldsymbol{\partial E}}{\boldsymbol{\partial t}}$$

1.4 Breakdown voltage

The most unique feature of power semiconductor devices is their ability to withstand high voltages. In transistors designed for microprocessors and semiconductor memories, the pressure to reduce their size to integrate more devices on a monolithic chip has resulted in a reduction in their operating voltage. In contrast, the desire to control larger power levels in motor drive and power distribution systems have encouraged the development of power devices with larger breakdown voltages.

Depending upon the application, the breakdown voltage of devices can range from 20 to 30 V for voltage regulator modules (power supplies) used to deliver power to microprocessors in personal computers and servers to over 5,000 V for devices used in power transmission networks. In a semiconductor, the ability to support high voltages without the onset of significant current flow is limited by the avalanche breakdown phenomenon, which is dependent on the electric field distribution within the structure.

High electric fields can be created within the interior of power devices as well as at their edges. The design optimization of power devices must be performed to meet the breakdown voltage requirements for the application while minimizing the on-state voltage drop, so that the power dissipation is reduced.

Power devices are designed to support high voltages within a depletion layer formed across either a P–N junction, a metal–semiconductor (Schottky barrier) contact, or a metal–oxide–semiconductor (MOS) interface. Any electrons or holes – that enter the depletion layer either due to the space-charge generation phenomenon or by diffusion from adjacent quasineutral regions – are swept out by the electric field produced in the region by the applied voltage. As the applied voltage is increased, the electric field in the depletion region increases, resulting in acceleration of the mobile carriers to higher velocities. In the case of silicon, the mobile carriers attain a saturated drift velocity of 1×10^{7} cm s^{-1} when the electric field exceeds 1×10^{5} V cm^{-1} With further increase in the electric field, the mobile carriers gain sufficient kinetic energy from the electric field, so that their interaction with the lattice atoms produces the excitation of electrons from the valence band into the conduction band. The generation of electron–hole pairs due to energy acquired from the electric field in the semiconductor is referred to as the *impact ionization*. Since the electron–hole pairs created by impact Ionization also undergo acceleration by the electric field in the depletion region, they participate in the creation of further pairs of electrons and holes. Consequently, Impact ionization is a multiplicative phenomenon, which produces a cascade of Mobile carriers being transported through the depletion region leading to a significant Current flow through it. Since the device is unable to sustain the application of higher voltages due to a rapid increase in the current, it is considered to undergo *Avalanche breakdown*. Thus, avalanche breakdown limits the maximum operating Voltage for power devices. the physics of avalanche breakdown is analyzed in relation to the properties of the semiconductor region that is supporting the voltage.

After treating the one-dimensional junction, the edge terminations for power devices are described. Power devices require special edge terminations due to their finite area. The electric field at the edges usually becomes larger than in the middle

of the Device leading to a reduction of the breakdown voltage. Significant effort has been Undertaken to develop a good understanding of the electric field enhancement at the edges and methods have been proposed to mitigate the increase in the electric Field. **[5]**

1.4.1 Avalanche breakdown

The maximum voltage that can be supported by a power device before the onset of Significant current flow is limited by the avalanche breakdown phenomenon. In A power device, the voltage is supported across depletion regions. Mobile carriers are accelerated in the presence of a high electric field until they gain sufficient energy to create hole–electron pairs upon collision with the Lattice atoms. This impact ionization process determines the current flowing through the depletion region in the presence of a large electric field. An Impact ionization coefficient as the number of electrons–hole pairs created by a mobile carrier traversing 1 cm through the depletion region along the direction of the electric field. The impact ionization coefficients for electrons and holes are a Strong function of the magnitude of the electric field as shown in figure 1.8 [**5]**

The impact ionization coefficient for holes (*αp*) is defined as the number of electron-hole pairs created by a hole traversing 1 cm through the depletion layer along the direction of the electric field. The impact ionization coefficient for electrons (*αn*) is defined as the number of electron-hole pairs created by an electron traversing 1 cm through the depletion layer along the direction of the electric field. **[6]**

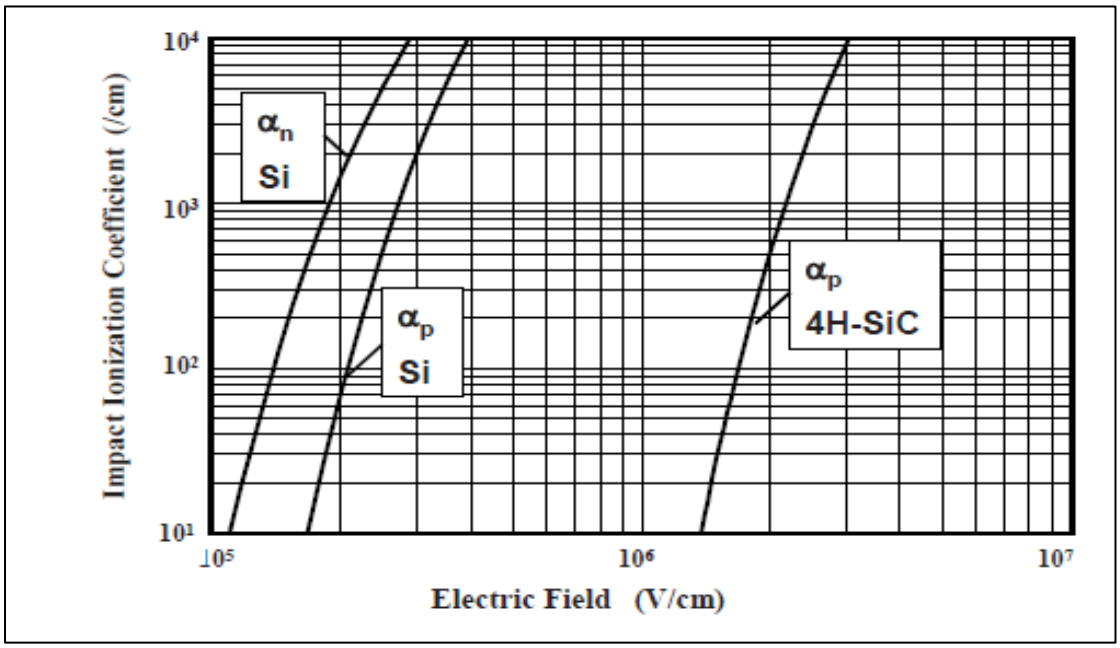


Figure1.7 *impact ionization coefficients for silicon and 4H-SiC*

1.4.2 Power law approximations for the impact ionization coefficients

It is convenient to use a power law, referred to as the *Fulop's approximation*:

$$\alpha_f \text{ (Si)} = 1.8 \times 10^{-35} E^7$$

for the impact ionization coefficients even though they actually increase exponentially with increasing electric field, when performing analytical derivations pertinent to the performance of silicon power devices. The impact ionization

coefficient obtained by using this approximation is shown in Fig. 1.7 by the dashed line together with the impact ionization coefficient for electrons in silicon as governed by the Chynoweth's law (shown by the solid line). In the same manner, it is convenient to use the *Baliga's power law approximation*2 for the impact ionization coefficients for 4H-SiC for analytical derivations:

$$\alpha_b(\text{4H-SiC}) = 3.9\times10^{-42}E^7$$

The impact ionization coefficient obtained by using this approximation is also shown in Figure.1.7 by the dashed line together with the impact ionization coefficient for holes in 4H-SiC as governed by the Chynoweth's law (shown by a solid line).

During numerical simulations of power device structures, it is customary to use the Chynoweth's formula for the impact ionization coefficients. However, the power law approximations are valuable for obtaining analytical solutions for the breakdown voltage of planar one-dimensional junctions and the influence of various edge terminations on the breakdown voltage. These analytical solutions provide insight into the physics determining the breakdown phenomenon, enabling the design of improved device structure.

1.4.3 Multiplication Coefficient

The avalanche breakdown condition is defined by the impact ionization rate becoming infinite. To analyze this, consider a one-dimensional reverse-biased N^+/P junction with a depletion region extending primarily in the P-region. If an electron–hole pair is generated at a distance *x* from the junction, the hole will be swept toward the contact to the P-region, while the electron is simultaneously swept toward the junction with the N^+ region. If the electric field in the depletion region is

large, these carriers will be accelerated until they gain sufficient energy to create electron–hole pairs during collisions with the lattice atoms. Based upon the definitions for the impact ionization coefficients, the hole will create [αp d*x*] electron–hole pairs when traversing a distance d*x* through the depletion region.

Simultaneously, the electron will create [α_n d*x*] electron–hole pairs when traversing a distance d*x* through the depletion region. The total number of electrons–hole pairs created in the depletion region due to a single electron–hole pair initially generated at a distance *x* from the junction is given by3,4 **[6]**

$$M(x)=1+\int_0^x \alpha n\, M(x)dx+\int_x^W \alpha p\, M(x)dx \qquad (2)$$

where *W* is the width of the depletion layer. A solution for this equation is given by

$$M(x)= M(0)\, \exp\left[\int^x (\alpha_n-\alpha_p)\, dx\right. \qquad (3)$$

where *M* (0) is the total number of electron–hole pairs at the edge of the depletion

region. Using this expression in (3.3) with *x* = 0 provides a solution for *M* (0):

$$M(0)=\{1-\int_0^W \alpha p\, \exp\left[\int_0^x (\alpha n-\alpha p)dx\right]\, dx\}^{-1} \qquad (4)$$

Using the expression in (2) gives:

$$M(x)= \frac{\exp[\int_0^x (\alpha n-\alpha p)dx]}{1-\int_0^W \alpha p\, \exp[\int_0^x (\alpha n-\alpha p)dx]\, dx} \qquad (5)$$

This expression for *M*(*x*), referred to as the *multiplication coefficient*, allows calculation of the total number of electrons–holes pairs created as a result of the generation of a single electron–hole pair at a distance *x* from the junction if the electric field distribution along the impact ionization path is known. The avalanche

breakdown condition, defined to occur when the total number of electrons–hole pairs generated within the depletion region approaches infinity, corresponds to *M* becoming equal to infinity. This condition is attained by setting the denominator of (4) to zero:

$$\{ \int_0^w \boldsymbol{\alpha p} \exp [\int_0^x (\boldsymbol{\alpha n} - \boldsymbol{\alpha p}) \boldsymbol{dx}] \boldsymbol{dx} \} = \mathbf{1} \quad (6)$$

The expression on the left-hand side of (3.7) is known as the *ionization integral*.

During the analysis of avalanche breakdown in power devices, it is common practice to find the voltage at which the ionization integral becomes equal to unity.

If the impact ionization coefficients for electrons and holes are assumed to be Equal, the avalanche breakdown condition can be write as

$$\int_0^w \boldsymbol{\alpha}\, \boldsymbol{dx} = \mathbf{1} \quad (7)$$

This approach to the determination of the breakdown voltage is valid for power rectifiers and MOSFETs where the current flowing through the depletion region is not amplified. In devices, such as thyristors and IGBTs, the current flowing through the depletion region becomes amplified by the gain of the internal transistors.

In these cases, it becomes necessary to solve for the multiplication coefficient instead of using the ionization integral. The multiplication coefficient for a high voltage P^+/N diode is given by

$$M_p = \frac{\mathbf{1}}{\mathbf{1} - (\frac{V}{BV})^6} \quad (8)$$

where *V* is the applied reverse bias voltage and BV is the breakdown voltage, while that for an N+/P diode is given by :

$$M_n = \frac{1}{1-(\frac{V}{BV})4} \quad (9)$$

Thus, the reverse current for a P+/N diode approaches infinity at a faster rate with increasing voltage than for an N+/P diode. This has been related to the diffusion current due to holes from the N-region in the P+/N diode.

1.4.4 Abrupt one-dimensional diode

Poisson equation for N region is given by:

$$\frac{d^2v}{dx^2} = -\frac{de}{dx} = -\frac{Q(x)}{\varepsilon s} = -\frac{qnd}{\varepsilon s} \quad (10)$$

Electric field distribution: $E(x) = -\frac{qnd}{\varepsilon s}$ (wd-x) (11)

Potential distribution: $V(x) = \frac{qnd}{\varepsilon s}$ (wd_x-$x^2/2$) (12)

V(wd)=Va

Depletion region width: $W_d = \sqrt{2\varepsilon s\, Va/qNd}$ (13)

Maximum electric field: $E_m = \sqrt{2qNdVa/\varepsilon s}$ (14)

The breakdown voltage is determined by the ionization integral becoming equal to unity:

$$\int_0^w \alpha \, dx = 1 \tag{15}$$

Substituting the Fulop's power law into the above equation together with the electric field distribution, analytical solutions for the breakdown voltage and the corresponding maximum depletion layer width can be derived for silicon:

$$BV_{pp}(si) = 5.34\times10^{13}\ N_d^{-3/4} \tag{16}$$

$$W_{pp}(si) = 2.67\times10^{10}\ N_d^{-7/8} \tag{17}$$

$$Ec(si) = 4010\ N_d^{1/8} \tag{18}$$

In a similar manner, substituting the Baliga's power law together with the electric field distribution, analytical solutions for the breakdown voltage and the corresponding maximum depletion layer width can be derived for 4H-SiC:

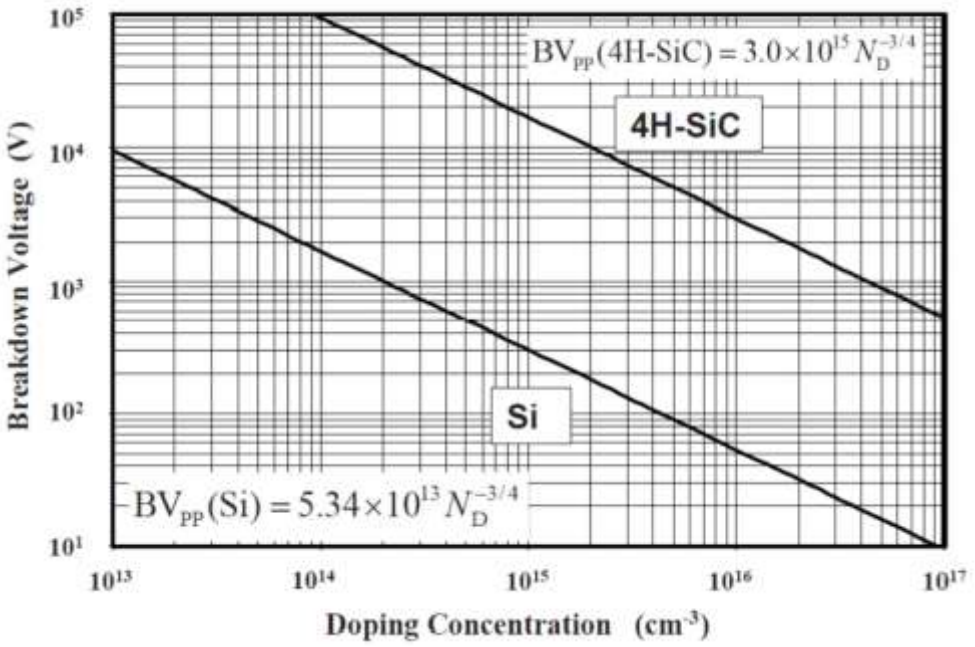


Figure1.8 *Breakdown voltage for abrupt parallel-plane junctions in Si and 4H-SiC*

$$BV_{pp}(4H\text{-}SiC) = 3.0\times10^{15}\ N_d^{-3/4} \quad (19)$$

$$W_{pp}(4H\text{-}SiC) = 1.82\times10^{11}\ N_d^{-7/8} \quad (20)$$

$$E_c(4H\text{-}SiC) = 3.3\times10^{4}\ N_d^{1/8} \quad (21)$$

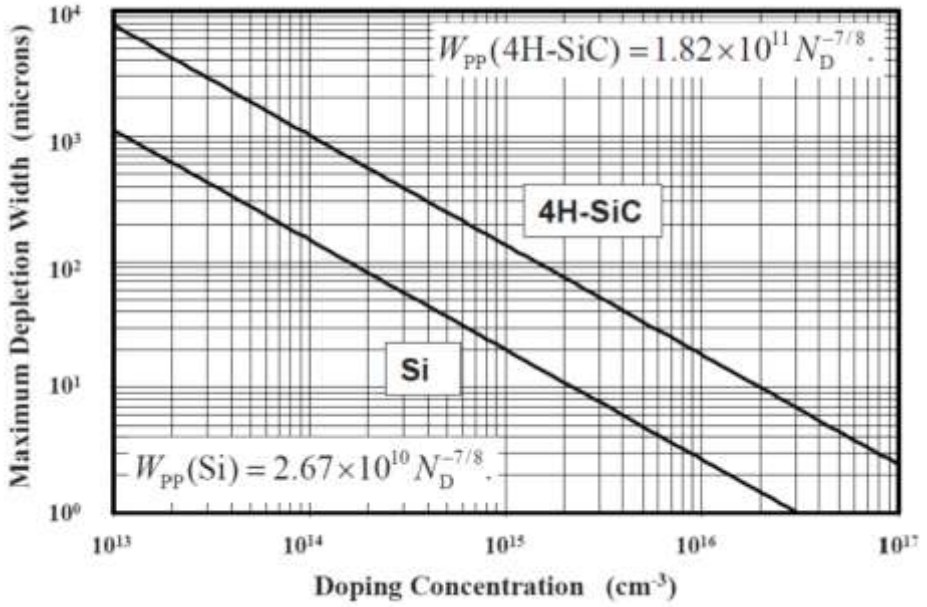


Figure1.9 *Maximum depletion width at breakdown in Si and 4H-SiC*

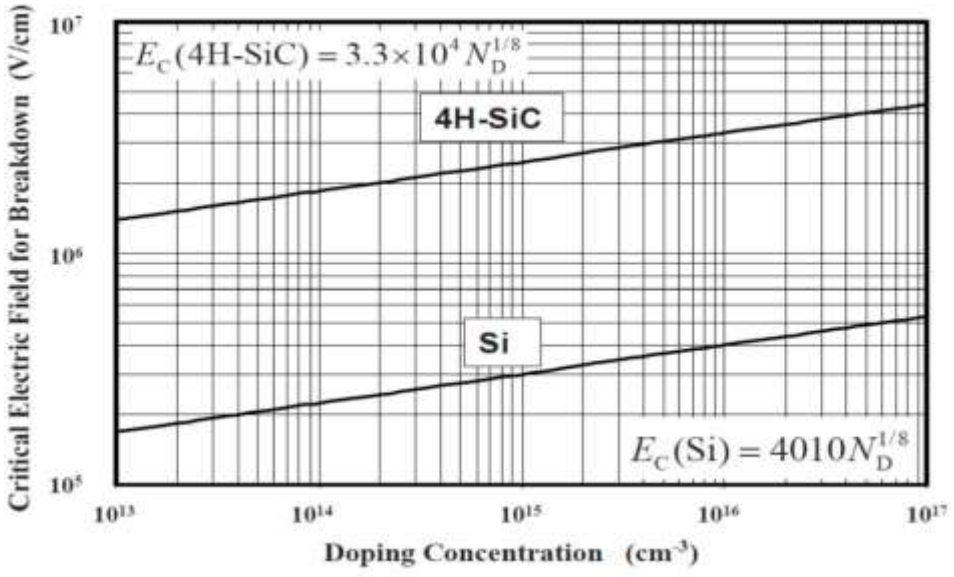


Figure1.10 *Electric Critical electric field for breakdown in Si and 4H-SiC*

1.5 Super junction

1.5.1 charge balance to explain the super junction effect

The RON limit of the 1-D design is clarified by these two equations:

$$\nabla.E = \frac{dE}{dx} = \frac{qND}{\varepsilon s} = \frac{Ec}{W} \quad (22)$$

$$BV = \frac{WEc}{2} \quad (23)$$

In order to increase the BV, it is mandatory to increase W and/or to reduce ND. Unfortunately, both actions result in increased RON.

The following imaginary experiment shows how to design an improved power device. The maximum BV for a given W is obtained with a flat electric field whose magnitude is Ec. The resulting, ideal BV for a given W, is: BV= WEc.

Equation (20) states that, in order to have a flat electric field, the doping of the epilayer should be zero. This means RON =∞ and hence the silicon limit has not been improved. Suppose that the epilayer is uniformly doped with a given concentration of p dopant and the same concentration of n dopant (this means that positive charges balance the negative charges) obtaining a device similar to the one shown in Figure (1.13) where the single dopants atoms are shown (n and p dopant atoms are green and red, respectively).

Such a sustaining layer behaves exactly like the intrinsic layer because the net charge is zero. The result is a flat electric field that maximizes the BV but the net charge equal zero also means that RON is still ∞.

Imagine that it is possible to align the n and p dopant atoms columnize on a microscopic scale, producing a device similar to the one shown in Figure(1.14)Because this is a minor modification that requires a small movement of the dopant atoms compared with Figure(1.13) , it is reasonable to assume that the

electric field is still flat and provides the ideal BV. With respect to RON, however, the situation is different. Because the ordered dopant atoms provide a low resistance path for the current flow, the resistance is no longer infinity. In this new configuration, the link between doping and dE/dx is broken and it is possible to design devices with very low RON. In conclusion, an SJ-sustaining layer improves the RON versus BV trade-off with respect to a conventional 1-D sustaining layer since the pillars contain positive and negative charges that balance each other. The resulting layer is similar to an intrinsic one with an almost flat electric field notwithstanding the resistance of the layer is very low.

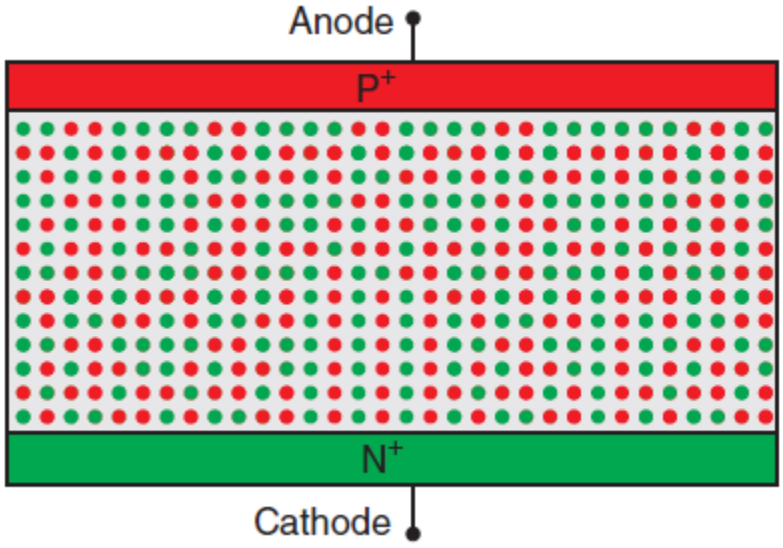


Figure1.11 *Conventional sustaining epilayer with n doping and p doping that sum to zero equivalent doping charge.*

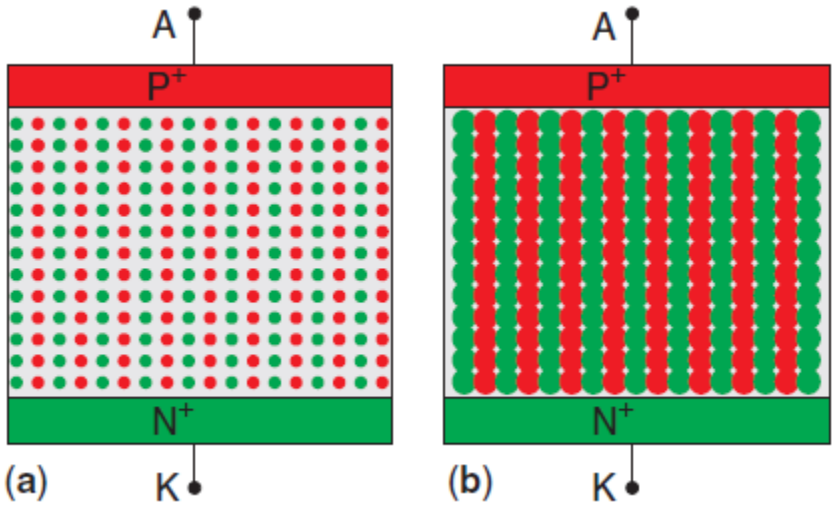


Figure1.12 *Aligning the dopants atoms column wise provides a favorable path for the current flow. (a) The aligned dopants and (b) the dopants form a series of adjacent pillars with alternating doping.*

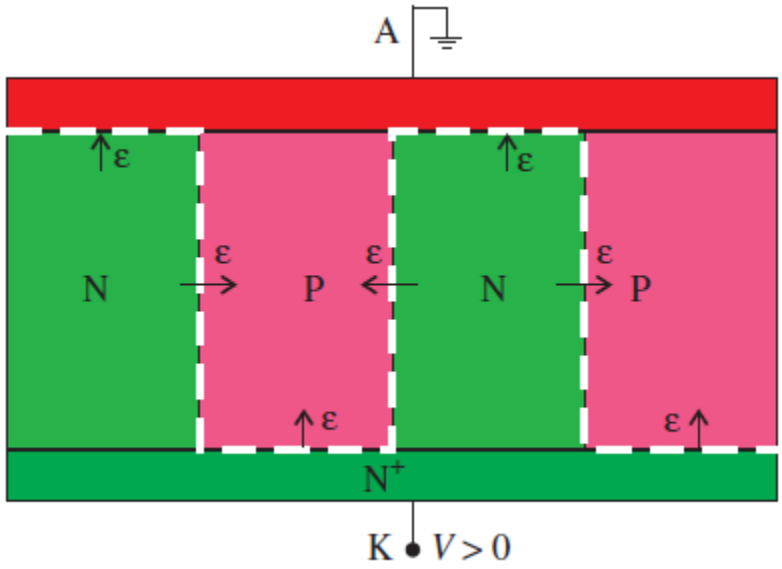


Figure 1.13 *SJ diode. The horizontal and vertical junctions are indicated with dashed line. The picture shows the main direction for the electric field also. Note the presence of an electric field in both horizontal and vertical directions.*

1.5.2 Design of superjunction devices

a What Is The Superjunction Structure?

Superjunction is a technique implemented in DMOS devices for the purpose of obtaining high breakdown voltage but with smaller on-resistance than the conventional device. In order to accomplish this, the drift region structure is modified and by doing this, the previous obstacle in the device identified as silicon limit is overcome. The superjunction drift region is composed of at least two oppositely doped pillars n and p, as opposed to the conventional device where the drift region is made out of only one type of doping. Actually, more than two pillars can be used when implementing the device This can have benefits over using just two, but certain conditions have to be taken into considerations.

To understand the reasons why this different structure works, an analysis on electric field and charge balance is needed.

b How does it work ?

A conventional sustaining layer is defined by two variables, the doping (ND) and the thickness (W). As a consequence, the optimal design rules for a given BV are fairly simple.

The SJ layer, as shown in Figure (1.14), is defined by five parameters: are the thickness (W), the doping for both pillars (ND, NA) and the width of the two pillars (YN, YP). It is therefore more difficult to define the design rule for the optimal design in SJ layers. One possibility is obtaining the optimal design through a time-consuming trial and error process based on 2-D numerical simulations. A better option is the use of accurate models for SJ behavior because the use of the models and of analytical relations is the only way to pillars that have unequal widths; slanted pillars; n and p pillars that have unequal doping. In this case, the rule of thumb for the design is guaranteeing the charge balance relation that is: $W_N N_D = W_{P\text{-}NA}$. **[3]**

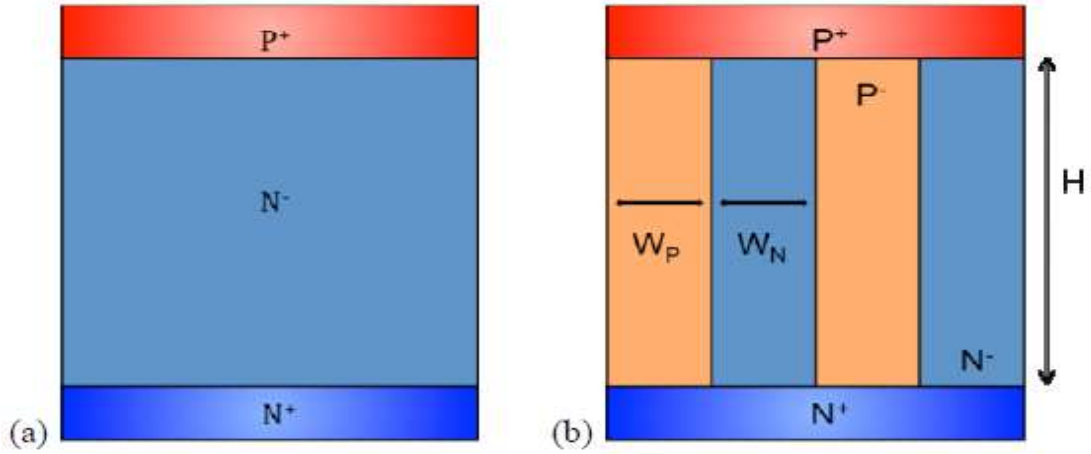


Figure1.14 *conventional diode and super junction diode.*

Two conditions must be satisfied for the super junction to work correctly:

- Band width W_N and W_P must be inferior to the length H.
- The bands N and P must respect a near perfect balance of loads.

1.6 Conclusion

In this chapter we are talking about notions of semiconductors and fundamental equations, we are defining the p-n junction specially in reversed biased to calculate the breakdown voltage and we are comparing the conventional diode with a super junction diode. in the next chapter we are represent the software of simulation that we have used in our study.

Chapter2. Silvaco Tools

2.1 Introduction

Silvaco TCAD can be applied to a breadth and depth of applications useful in the development of semiconductor technologies. TCAD has been proven to be a powerful tool to provide in-depth understanding of device fabrication and operation. When applied by engineers to their Semiconductor R&D needs, TCAD can provide insights difficult or even impossible to achieve empirically. TCAD can help enhance device performance, increase yield and reduce time to market.

However, applying TCAD is a complex learned skill and engineers must apply their own skill and experience as a solid-state physicist, electrical engineer or circuit designer. Applying that knowledge to harness the TCAD infrastructure will their simulation goals to be achieved. TCAD software combines industry and academic physics knowledge, advanced numerical methods, user interfaces, and automation to allow engineers to get the answers they need.**[7]**

There are other simulators in the market (SYNOPSIS, SILVACO, ISE, etc. ...) with the same operating principle. In this project, we will be using the TCAD-SILVACO.

In this chapter, we present the simulation software " Silvaco " and it's functioning tools, as for our project we used the simulation module ATLAS to simulate the electric characteristic of simple pin junction, a trench junction & compare it with the super junction type. But first we need to know some basic notions about the simulation in general & of this software in particular, with some examples to illustrate the work.

2.2 Silvaco

2.2.1 ATHENA

Athena is a simulator that provides general capabilities for numerical, physically-based, two-dimensional simulation of semiconductor processing; has a modular architecture that the following licensable tools and extensions:

•**ATHENA**: This tool performs structure initialization and manipulation, and provides basic deposition and etch facilities

•**SSUPREM4**: This tool is used in the design, analysis, and optimization of silicon semiconductor structures. It simulates silicon-processing steps such as ion implantation, diffusion and oxidation.

•**ELITE**: This tool is a general-purpose 2D topography simulator that accurately describes a wide range of deposition, etch and reflow processes used in modern IC technologies.

•**OPTOLITH**: This tool performs general optical lithography simulation including 2D aerial imaging, non-planar photoresist exposure, and post exposure bake and development. [8]

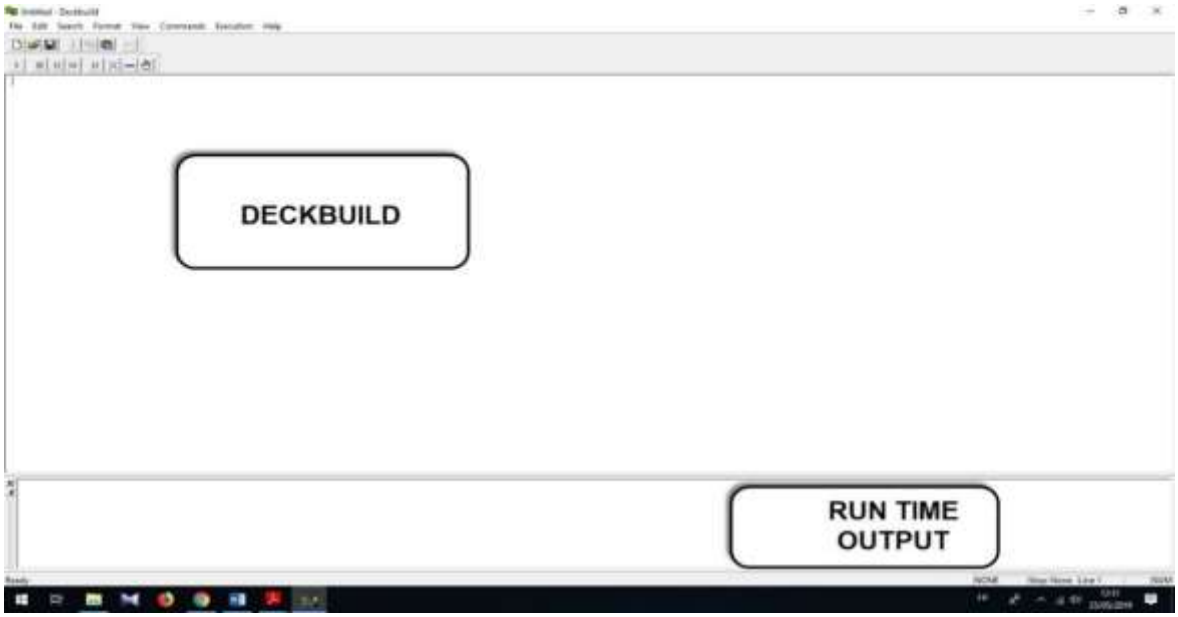


Figure.2.1 DeckBuild Tool

DeckBuild is an interactive runtime and input fi le development environment within which all Silvaco's TCAD and several other Silvaco products can run. DeckBuild has numerous simulator specific and general debugger style tools, such as powerful extract statements. It contains an extensive library of hundreds of pre-run examples decks which cover many technologies and materials.

2.2.2 DEVEDIT

It can be used to either create a device from scratch or to re-mesh or edit an existing device. DevEdit creates standard Silvaco structures that are easily integrated into Silvaco 2D or 3D simulators and other support tools.

2.2.3 TONYPLOT

TonyPlot is a powerful tool designed to visualize TCAD 1D and 2D structures produced by Silvaco TCAD simulators. TonyPlot provides visualization and graphic features such as pan, zoom, views, labels and multiple plot support. TonyPlot also provides many TCAD specific visualization functions such as HP4154 emulation, 1D cut lines from 2D structures, animation of markers to show vector flow, integration of log or 1D data files and fully customizable TCAD specific colors and styles.

2.2.4 ATLAS :

ATLAS is a modular and extensible framework for one, two and three dimensional semiconductor device simulation. It is implemented using modern software engineering practices that promote reliability, maintainability, and extensibility. Products that use the ATLAS Framework meet the device simulation needs of all semiconductor application areas.

It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation.

2.3 Using ATLAS

2.3.1 Atlas inputs and outputs

We 'll be conducting our study using the simulator model "ATLAS" which was designed in a way that ease usage of other tools as shown in the figure below.

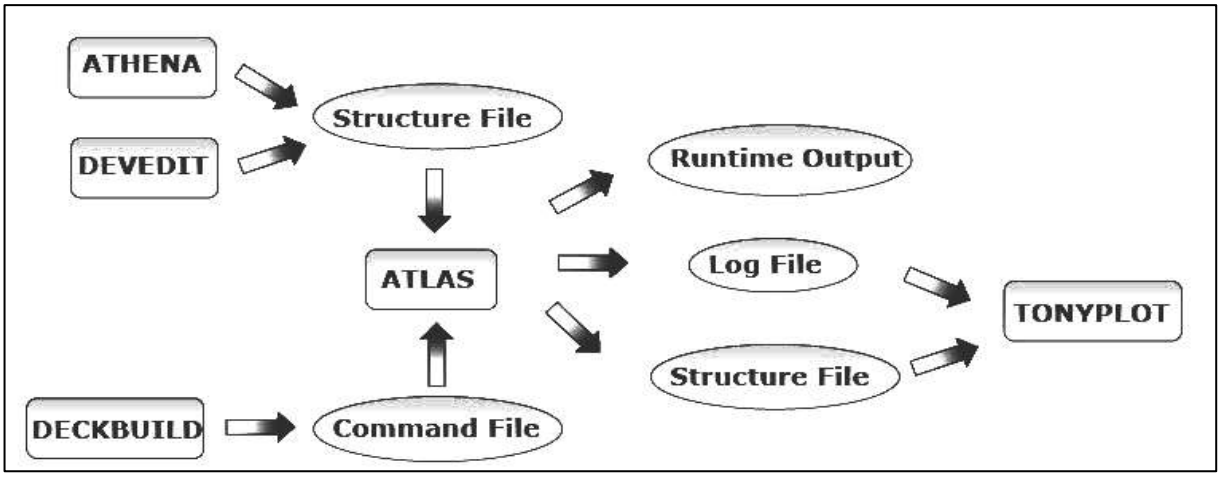


Figure2.2 Atlas Inputs and Outputs.

Atlas uses two type of input file:

-The first file is a text file that contains Atlas's commands (command file). -As for the second file, it defines the structure to be simulated (structure file).

Atlas produce three types of output file:

-The runtime output that gives error and warning messages as the simulation proceeds.

-The log file that stores voltages and currents.

-The structure file that stores 2D and 3D data relating to the values of solution variables (solution file).

2.3.2 The Order of ATLAS Commands :

Group	**Statement**
1.Structure Specification	▪ MESH ▪ REGION ▪ ELECTRODE ▪ DOPING
2.Material Models Specification	▪ MATERIAL ▪ MODELS ▪ CONTACT ▪ INTERFACE
3.Numerical Method Selection	▪ METHODE
4.Solution Specification	▪ LOG ▪ SOLVE ▪ LOAD ▪ SAVE
5.Results Analysis	▪ EXTRACT ▪ TONYPLOT

Table2.1 Order groups in ATLAS with their primary declaration in each group.

2.3.3 1.Structure Specification:

a Mesh specification

……..

MESH SPACE .MULT=<VALUE>

This instruction is used to define the vertical lines (y axis) & the horizontal ones (X axis) spaced from each other .The mesh that being made in our study is two- dimensional (2D),that way we'll only define the X & Y parameters.

SPACE.MULT is a multiplication factor between two mesh lines define by the spacing instruction in a given direction to decrease or increase the number of mesh lines.

the instruction that defines the mesh is written as follows :

X.MESH LOCATION=<VALUE> SPACING=<VALUE>

For example:

x.m l=3 spac=0.1

x.m l=6 spac=0.5

x.m l=9 spac=0.1

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>

Note:

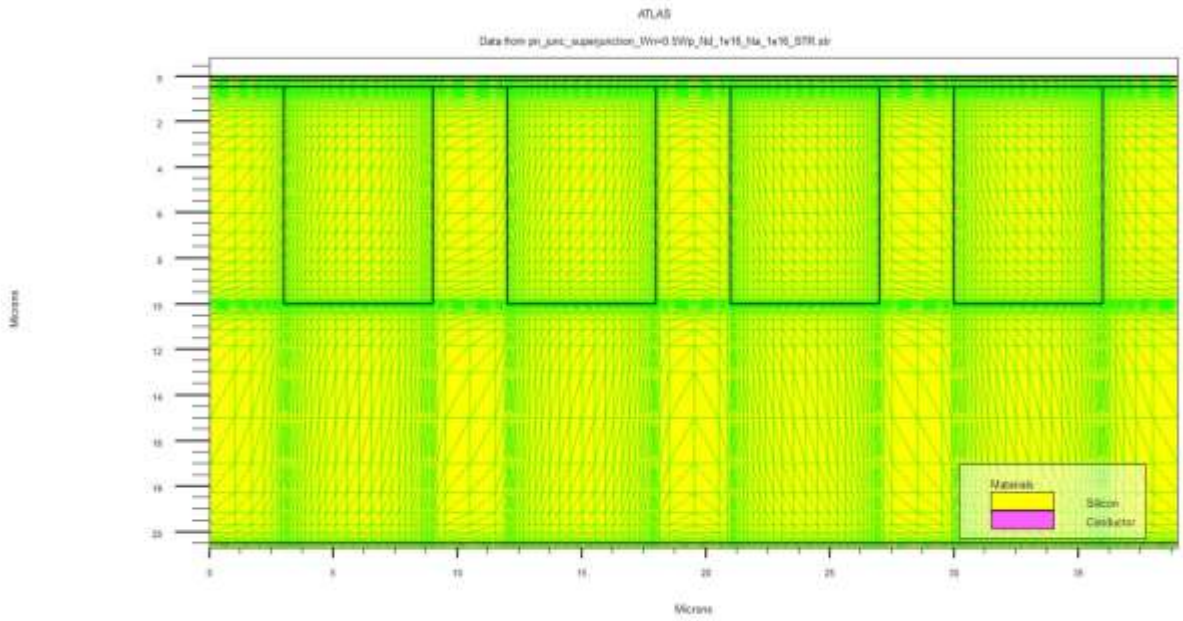
x.mesh defines the mesh in direction of the X.

y.mesh defines the mesh in direction of the Y.

l defines the location of the mesh.

Spac define the mesh resolution.

The approximation or the distance from the mesh lines is a crucial step during the simulation. It will be decisive for the accuracy of the results and the speed of calculation time. The designer must make a compromise between the two parameters.



.**Figure 2.3** Structure represent the horizontal and the vertical grid.

The input file contains a sequence of statements. Each statement consists of a keyword that identifies the statement and a set of parameters. In ATLAS the general format is :

<STATEMENT> <PARAMETER>=<VALUE>

The statement keyword must come first but the order of parameters within a statement is unimportant. we only need to use enough letters of any parameter to distinguish it from any other parameter on the same statement. Thus, CONCENTRATION can be shortened to CONC. REGION. It can't be shortened to R.

ATLAS can read up to 256 characters on one line. But it is better to spread long input statements over several lines to make the input file more readable. The (antislash) **** character at the end of a line indicates continuation.

Any line beginning with a **#** is ignored. These lines are used as comments.**[9]**

b Région specification

The statement that permit to specify the region of a structure is defined as follows

REGION number=<integer> <material_type><position parameters>

The regions must be defined by the following instruction just after the Mesh definition.

This instruction state the region name & number, as well as the type & position of the material through the parameters of x and y.

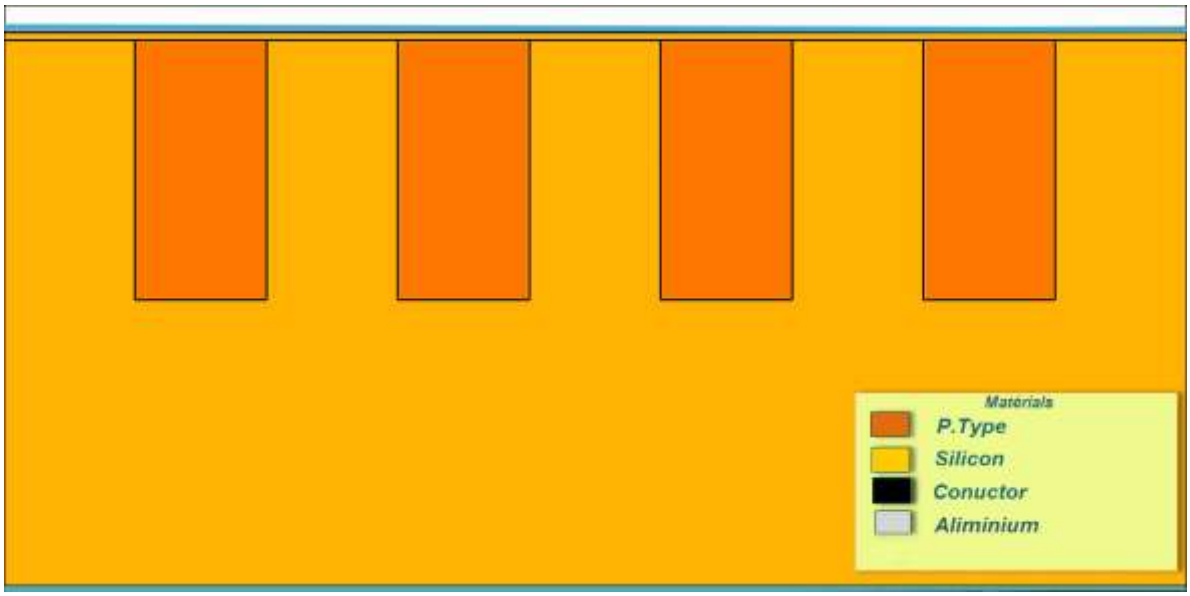


Figure2.4 *The different regions in a super-junction.*

c Electrode specification

The statement that permit to define the structure's electrodes is the following **ELECTRODE NAME=<electrodename> <position_parameters>**

Up to 50 electrodes and more can be specified, electrode positions are localized by

The following instructions:

X.MIN: Specifies the starting point of the electrode.

RIGHT: The position of the electrode is to the right of the structure (inverse: LEFT).

TOP : The position of the electrode is at the top of the structure (inverse: BUTTOM).

In our study, we only have two electrodes, an anode at the top of the structure and a cathode at the bottom of the structure translated by the following instructions:

electrode name=anode top

electrode name=cathode bottom

The figure shows the two electrodes:

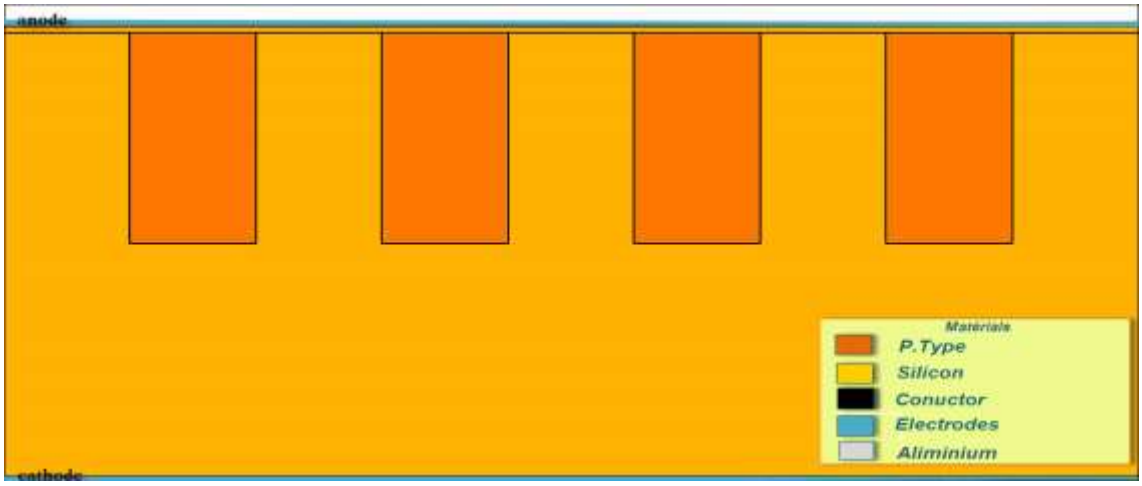


Figure2.5 The electrodes in a super-junction structure.

d Doping specification

Doping is defined by the following instruction:

DOPING <distribution_type><dopant_type><position_parameters>

This instruction makes it possible to declare the doping distribution, which we have chosen. In our study, we chose the doping's uniform distribution, type & position.

For example:

```
# epi- n doping
doping uniform n.type conc=$Nd region=1

# Junction doping
doping uniform p.type conc=$Na region=3
doping uniform p.type conc=$Na region=4
```

backside substrate : n++ doping (ohmic contact)

doping uniform n.type conc=1e+20 region=2

Once the structure is defined, you can save this information in a file of type ”str”.

This can be accomplished by the following statement:

save outf =$’filename’_STR.str

We can also visualize the diagram of the structure with the help of TONYPLOT tool by using the following instruction:

tonyplot $'filename'_STR.str

2.3.4 specification of materials and physical models

After the specification of the mesh and the doping, we move to the next step where one can easily modify the characteristics of the materials used (electrodes, substrate).

These actions are accomplished by the following instructions:

CONTACT, MATERIAL & MODELS.

a Material specification

All materials are classified according to their physical properties such as (conductivity, electronic affinity, gap energy & Mobility …etc).

The MATERIAL instruction allows to associate the physical parameters with the materials used in the simulation.

b Model specification

All physical models are specified by both MODELS and IMPACT statements.

These instructions makes it possible to use the existing physical models in the Software.

Some of the models :

- The dependence of the mobility as a function pg the concentration of the carriers introduces the model **CONMOB.**
- The dependence of the mobility of the electric field by **FLDMOB**.
- The recombinant generation factor by **SRH. [10]**

The choice of model depends on the materials chosen in the simulation.

For example :

models kla fldmob conmob consrh auger fermi bgn trap.tunnel

impact selb.

« **impact Selb** » this model is recommended for most cases, it is used in general for the reverse polarization.

c Contacts specification

This instruction indicates the physical attributes of an electrode. It is defined as follow:

CONTACT number= < n > | NAME=<name>

Example:

contact name=anode

If an electrode is in contact with a semiconductor, by default, ATLAS recognizes it as an ohmic contact.If the WorkFunction statement, specifying the work output as eV, is added, the contact is considered as a Schottky contact. **[10]**

d Interface specification

This instruction allows to indicate interface parameters at semiconductor or insulator boundaries, it is not useful in our study as we did not use several materials. So, at the surface we do not have variations of recombination and charge density.

The command «Output» is used to display the different information, for example: The electron current of the holes, the electric field.....etc.

Example:

output j.electron j.hole j.conduc j.total e.field ex.field ey.field flowlines \

e.mobility h.mobility e.temp h.temp qss charge recomb.

2.3.5 Numerical methods

Several different numerical methods can be used for calculating the solutions to semiconductor device problems. After the complete specification of the structure (geometry and physics) ATLAS begin to solve a series of equations (continuity equations, fish equation, equations of diffusion) to calculate carrier densities, potentials and currents.

Different combinations of models will require ATLAS to solve up to six equations. For each of the model types, there are basically three types of solution techniques:

-decoupled (GUMMEL).

-fully coupled (NEWTON.

-BLOCK.

a Gummel

The GUMMEL method will solve for each unknown in turn keeping the other variables constant, repeating the process until a stable solution is achieved. Generally, the GUMMEL method is useful where the system of equations is weakly coupled but has only linear convergence.

b Newton

The NEWTON method solve the total system of unknowns together, The NEWTON method may, however, spend extra time solving for quantities, which are essentially constant or weakly coupled. NEWTON also requires a more accurate initial guess to the problem to obtain convergence.

c Block

The BLOCK methods will solve some equations fully coupled while others are de-coupled. It can provide for faster simulations times in these cases over NEWTON.

2.3.6 Specification of solutions

This step allows to specify the solution after finishing the selection of the numerical Methods. this specification is composed by these commands : LOG,SOLVE,LOAD,& Save.

a Log

This declaration makes it possible to record all the electrical quantities in a file as shown in the following instruction:

```
set     IVR = $'filename'_IVR

LOG     outfile = $'IVR'.log
```

b Solve

This command SOLVE follows the instruction **log** .which makes it possible to carry out a solution for one or more point of polarization as the following format shows it:

```
SOLVE   vanode=-0.2  vstep=-0.2  vfinal=-1   name=anode
SOLVE                vstep=-1    vfinal=-5   name=anode
SOLVE   vstep=-1     vfinal=-200 name=anode compliance=-1e-09 cname=anode
```

There are two methods to stop the simulation «vfinal» «Compliance», the latter is intended to force the stop for a specified current value.

c Load

This command loads a structure with all its previous solutions in order to use it later.The instruction is given as follows :

```
LOAD    infile =  $'IVR'_5V.str          master
```

d Save

The save command allows you to save all information that corresponds to a specific electrical state.The save statement is :

SAVE outfile = $'IVR'_5V.str

SAVE outfile = $'IVR'_20V.str

2.3.7 Results analysis

The results can be displayed graphically from the «Tonyplot» instruction and the device parameters can be extracted from the «Extract» instruction.

a Extract

An instruction that can extract different parameters such as Breakdown Voltage, leakage current & IVR…etc. It's written as follows:

EXTRACT init infile = "$'filename'.log"

EXTRACT name="V_Breakdown" x.val from curve(abs(v."anode"), abs(i."anode"))

where y.val=1e-10 \ datafile="$'filename'_IVR_VBD_values.dat"

From the given curve, this instruction makes it possible to extract a BV for a certain value of y. where « y » axis refers to the courant ,and the « x » axis represent the voltages.

b TonyPlot

This command is used to display structures and results as a graph the instruction to do that is as follows

TonyPlot $'filename'_STR.str

TonyPlot $'IVR'.log

2.4 Conclusion

In this chapter we are presenting the Silvaco TCAD software .it contains many simulation model, each model has its own properties. In our study, we used the ATLAS simulation tools and how to configure its different parameters.

We defined every model we used in our simulation in general, in order to use it later in chapter three. In the next chapter we represent the simulation results which we used in our studies.

Chapter3. **Results**

3.1 *Introduction*

In this chapter we'll expose the main results obtained in the simulation as well as the methodology adopted concerning the performance of a super junction diode by applying different parameters, in order to obtain the highest possible stable breakdown voltage of a diode -type semiconductor.

The geometry, doping, as well as the reversed tension on current-voltage characteristics will also be studied. Finally, a comparison with the experimental results obtained.

Before starting the simulations for our experimental structures, we have simulated a conventional diode structure, another diode with deep trench and the structure to be studied (super junction) by modifying some technological and geometric parameters.

3.2 *Device Structure*

*Th*e figure 3.1 represents the diagram of the optimal structure that we studied. All technological and geometric parameters are grouped in the table 3.1

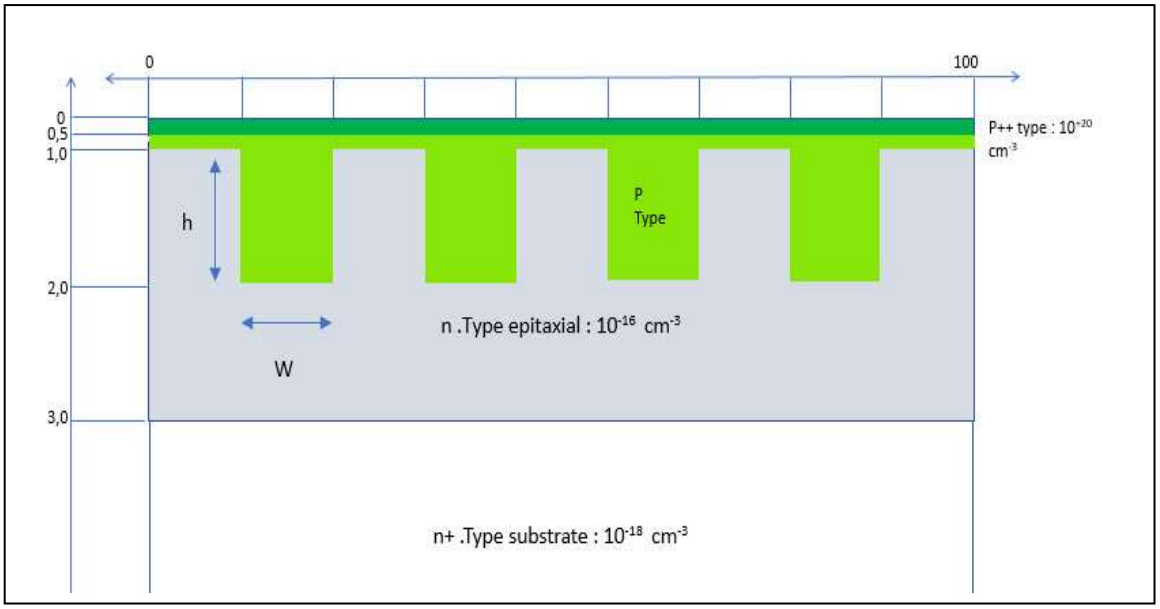


Figure3.1 *Super junction Structure used in Our Study.*

Structure parameters	***Values***
Substrate doping (n type) epitaxial	$10^{+16}\ cm^{-3}$
Substrate doping (n+ type)	$10^{+18}\ cm^{-3}$
Trench doping (p type)	$10^{+16}\ cm^{-3}$
The width of the substrate	*100µm*
Substrate depth	*20µm*
Junction depth (p type)	*0.5µm*
Trench width (optimum)	*4 µm*
Trench depth (optimum)	*10 µm*
Anode (p++ type)	$10^{+20}\ cm^{-3}$
Cathode (n++ type)	$10^{+20}\ cm^{-3}$

Table3.1 *Different values for structure's parameters.*

3.2.1 *Conventional structure*

*This structure represents a simple **p n** junction. The figure 3.1 shows the electrical potential, the intensity of the electric field as well as the electron's concentration. The graphs are obtained by a cross section at the p-n junction. By applying a reversed biased voltage (50V), we notice at first that the potential decreases quickly, the same goes for the electric field at the edge of the **p n** junction. However, the electrons concertation increases aggressively at the terminals of the junction, then stabilize at a certain point.*

The figures 3.3a),b) and c) represents the potential profile, the electric field, and the electron concentration, respectively.

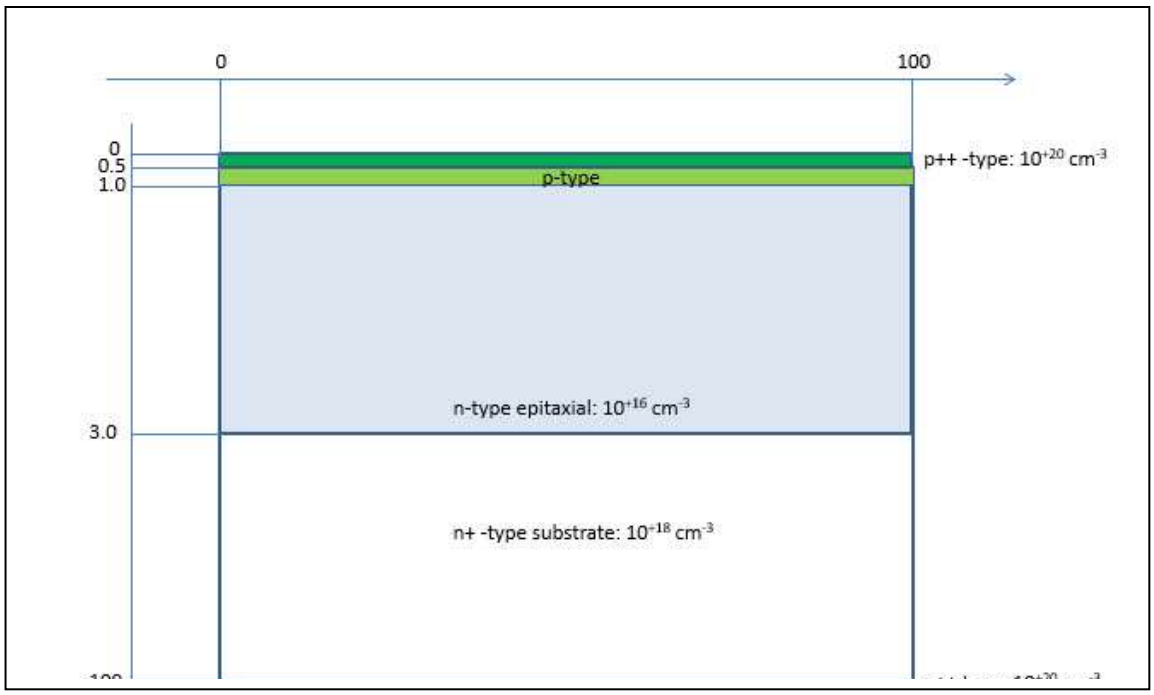


***Figure**3.2 Conventional junction Structure.*

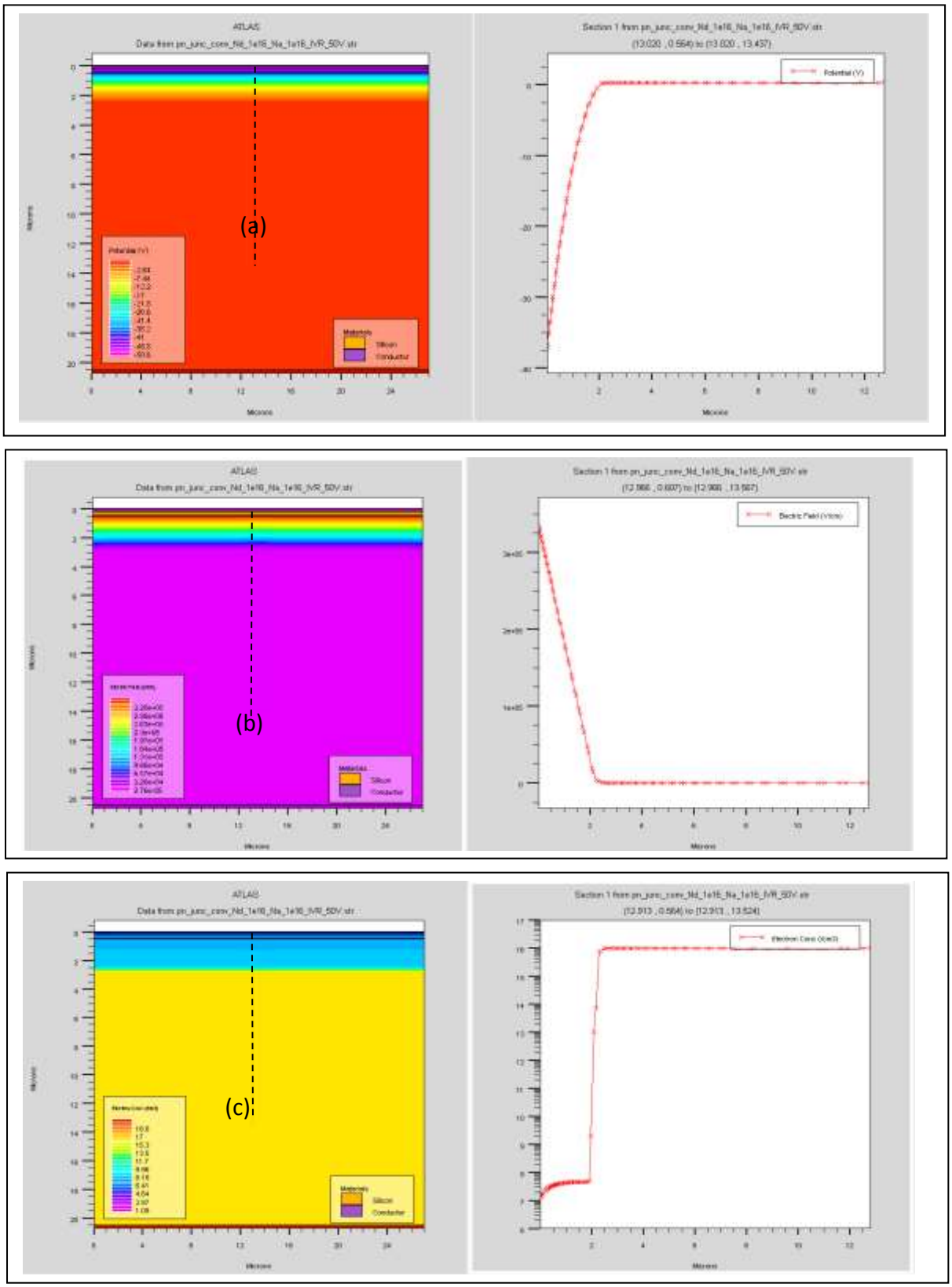


Figure3.3 *Cutline of The electrical potential, the intensity of the electric field and the electron's concentration in a conventional junction reversed biased at 50 V.*

3.2.2 *Trench*

This structure represents a trench-type junction. The figure 3.5 shows the electrical potential, the intensity of the electric field as well as the electron's concentration. The graphs are obtained by a cross section at the p-n junction.

The results obtained for a trench type junction are similar to those of a conventional pin diode, therefore, throughout the simulation, these results are omitted

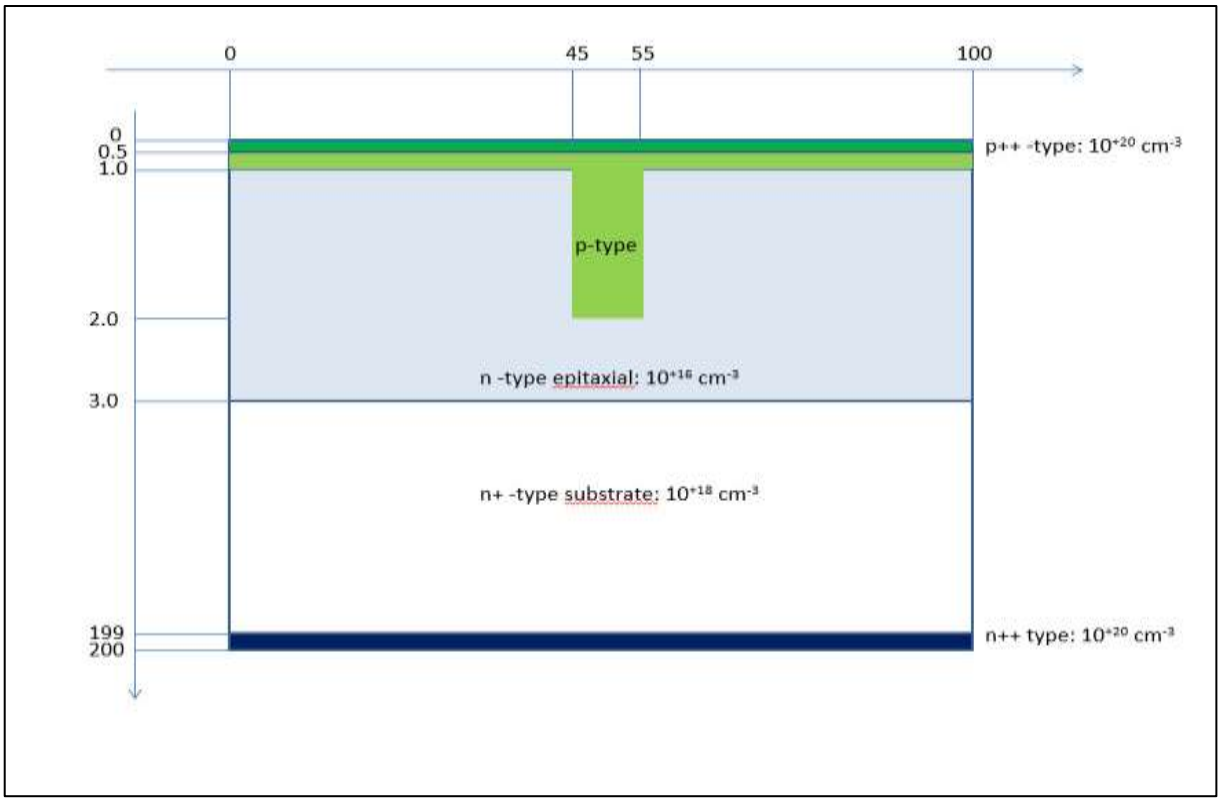
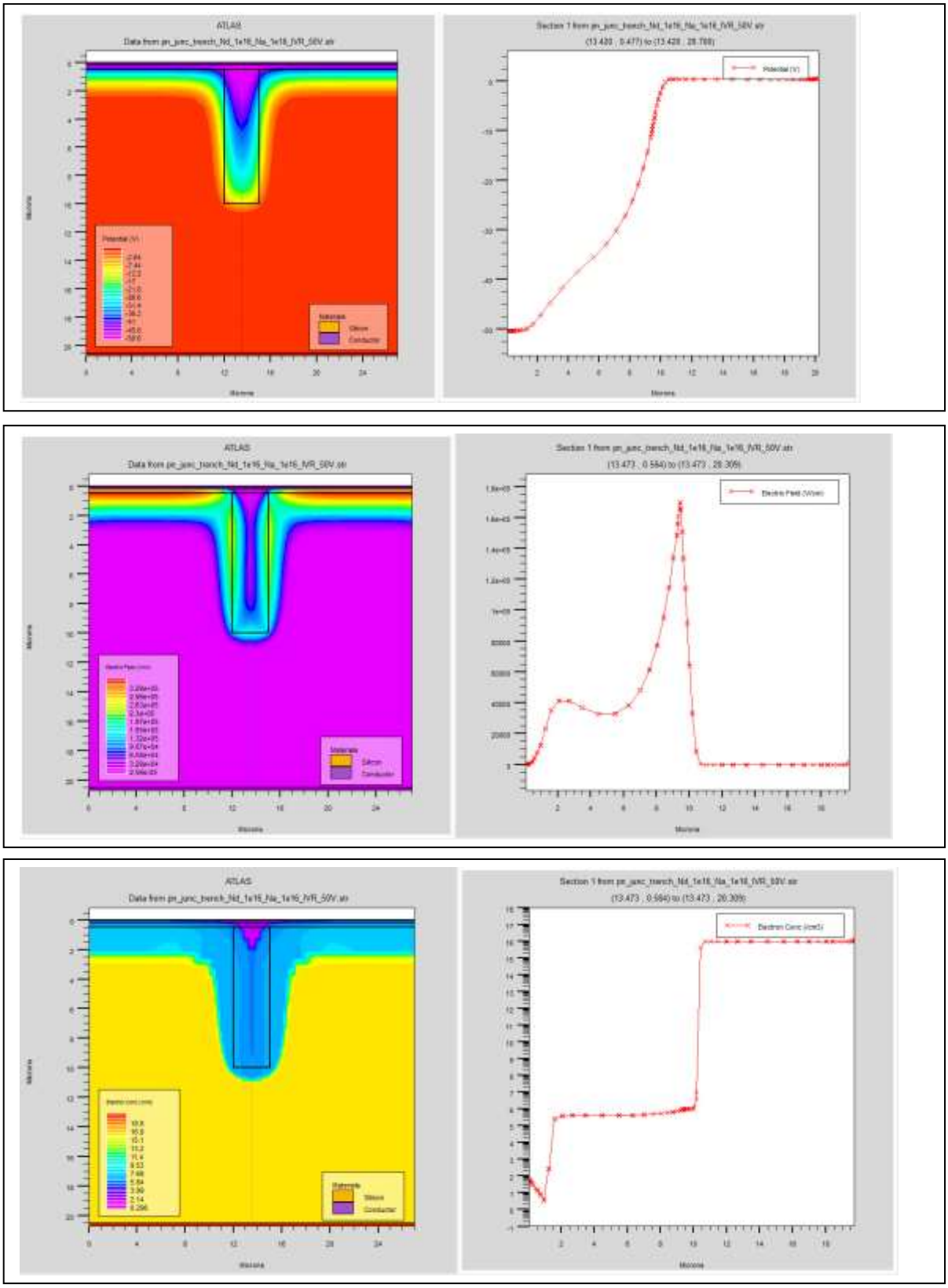


***Figure**3.4 Trench-type junction Structure.*



***dFigure**3.5 The electrical potential, the intensity of the electric field and the electron's concentration in a trench-type junction reversed biased at 50 V*

.

3.2.3 *Super junction*

This structure in figure 3.6 has many trenches which defines the super junction model in semiconductor of diode type (p-n junction).The figure 3.7 shows that SJ has the highest breakdown voltage for a small applied revered biased tension (20V).

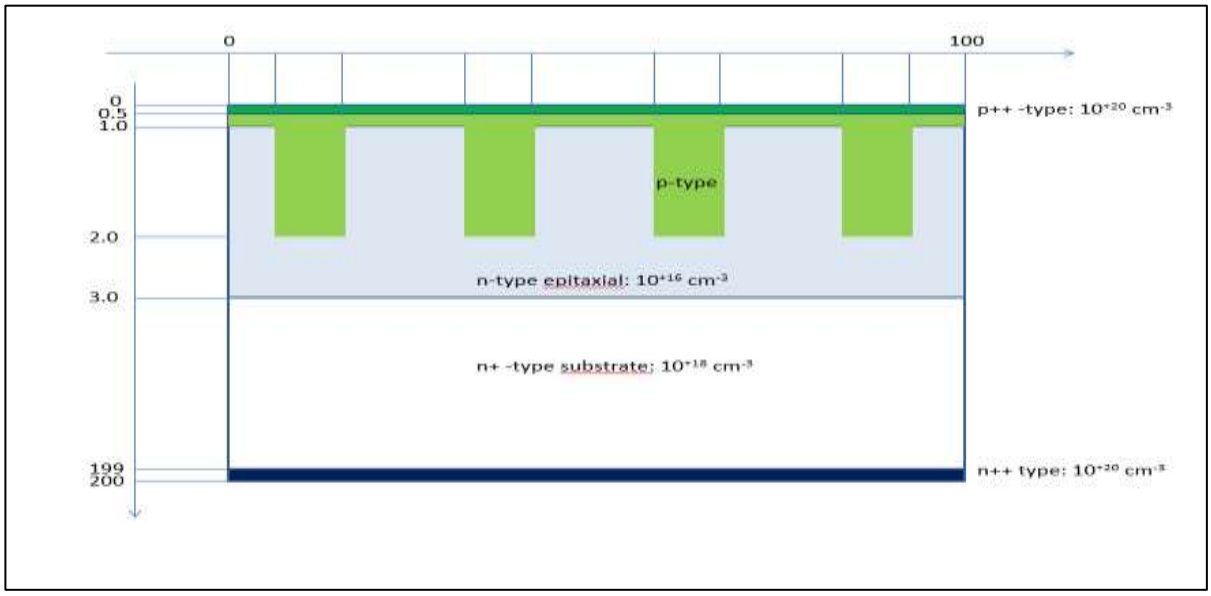


Figure3.6 *Super junction Structure.*

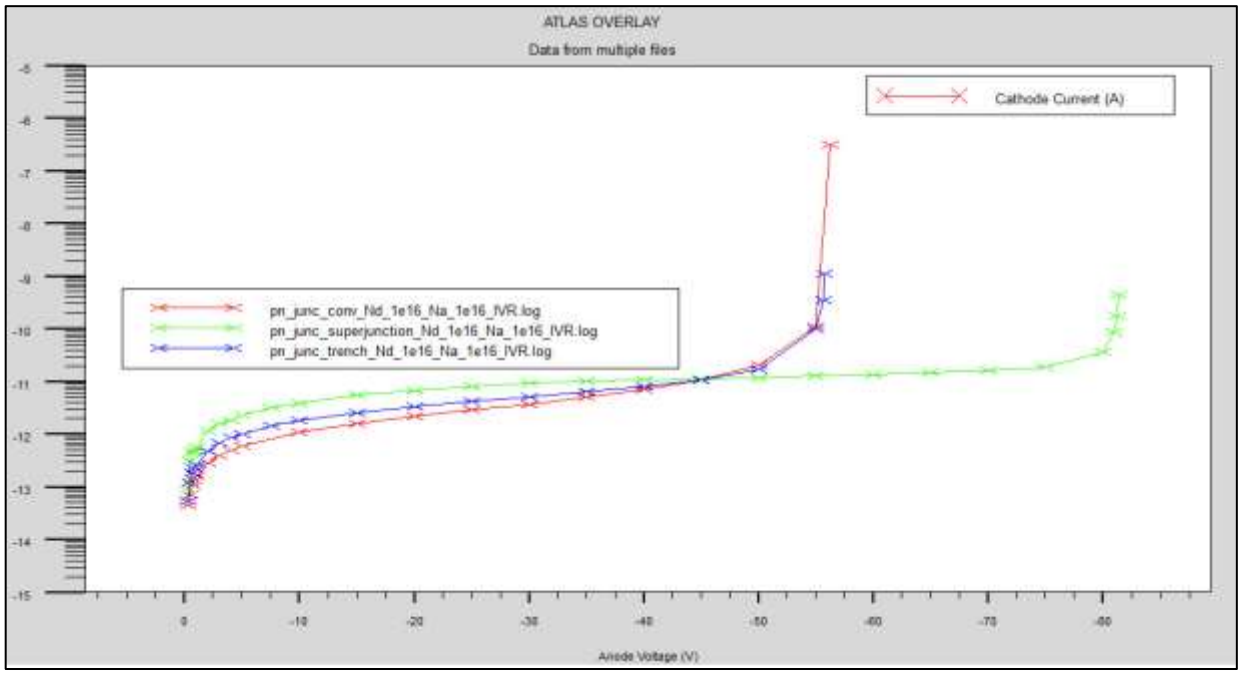


Figure3.7 *Super junction Bv compared to the Conventional and trench type.*

3.2.4 *Geometric optimization*

This optimization consists in finding the optimal position according to x a y (width & depth) of the trenches in a super junction n-p reversed biased, for that we are going to simulate our structure by varying it's three basic parameters

(Width: Wn Wp, Depth: H, Doping: Na ,Nd)
Starting with :

a Width variation

*The figure 3.7 shows a number of super junction structures with different width that we used in our study. Variation between **Wn** and **Wp** allow us to determine which optimal width is to be chosen to obtain a high breakdown voltage.*

The table 3.2 clearly shows that to score a high BV using a Super junction structure, requires to have equal width for both substrate (n type) and trenches (p type) .the resukts are illustrated in the figure 3.8.

Width	Wn=0.5Wp	Wn=Wp	Wn=2Wp	Wn=3Wp
BV	95 V	170 V	75V	55V

Table3.2 BV values for different Wn & Wp width

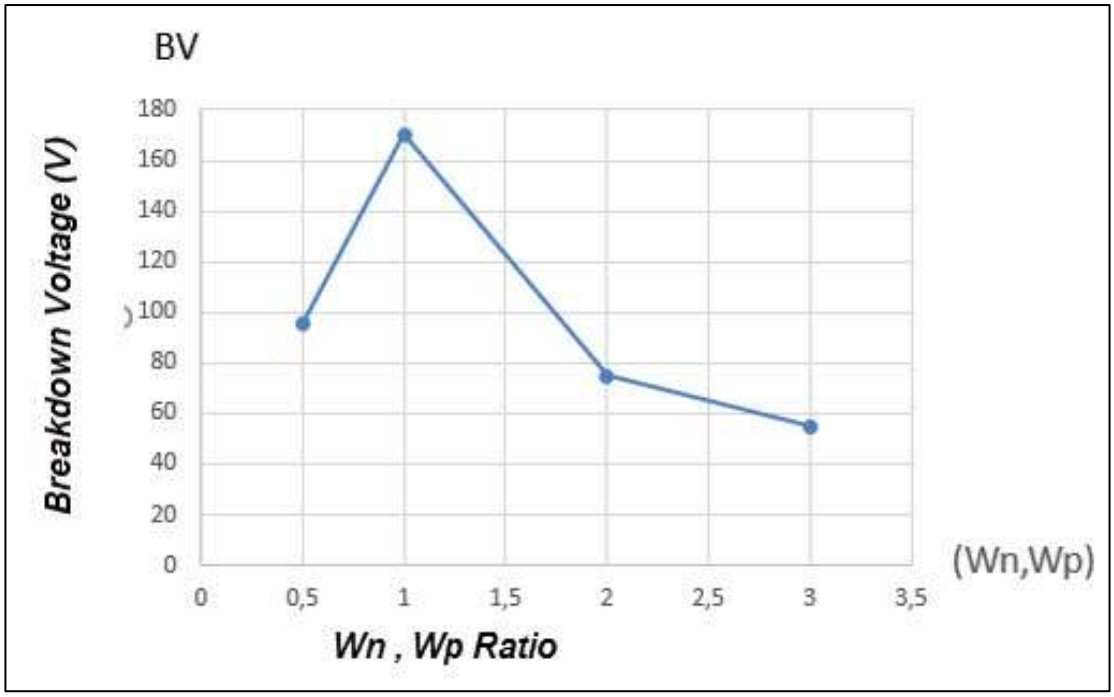


Figure3.8 *Breakdown voltage according to trench width.*

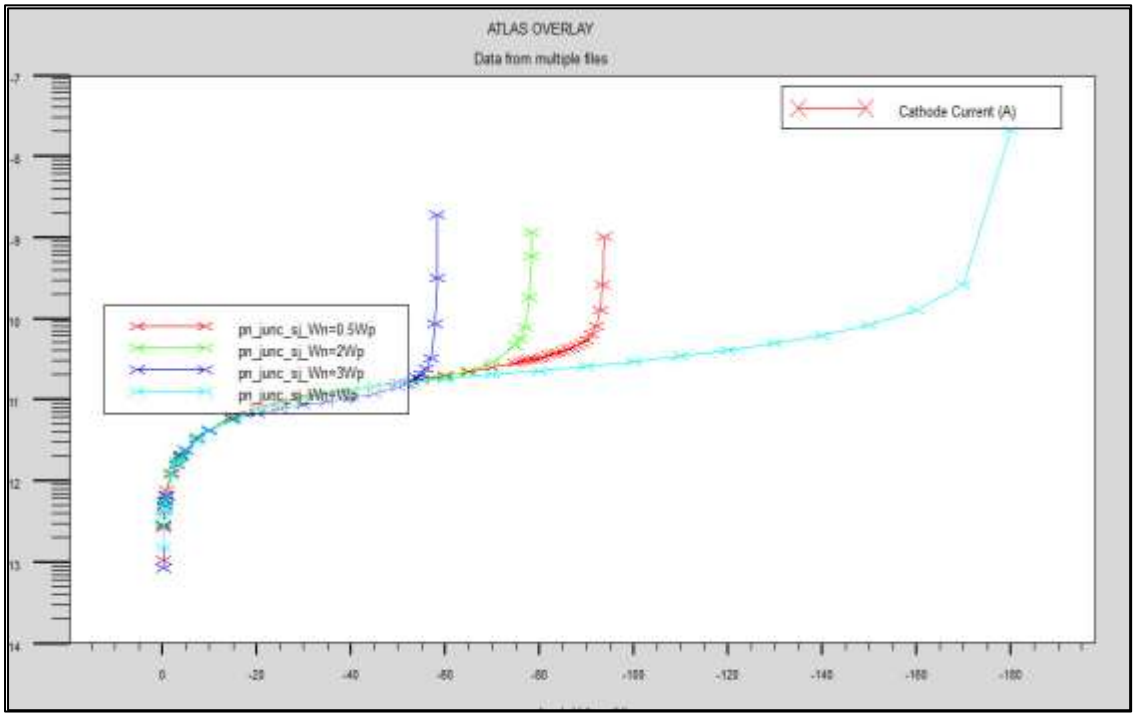


Figure3.9 *Breakdown voltage for variation of Wn and Wp.*

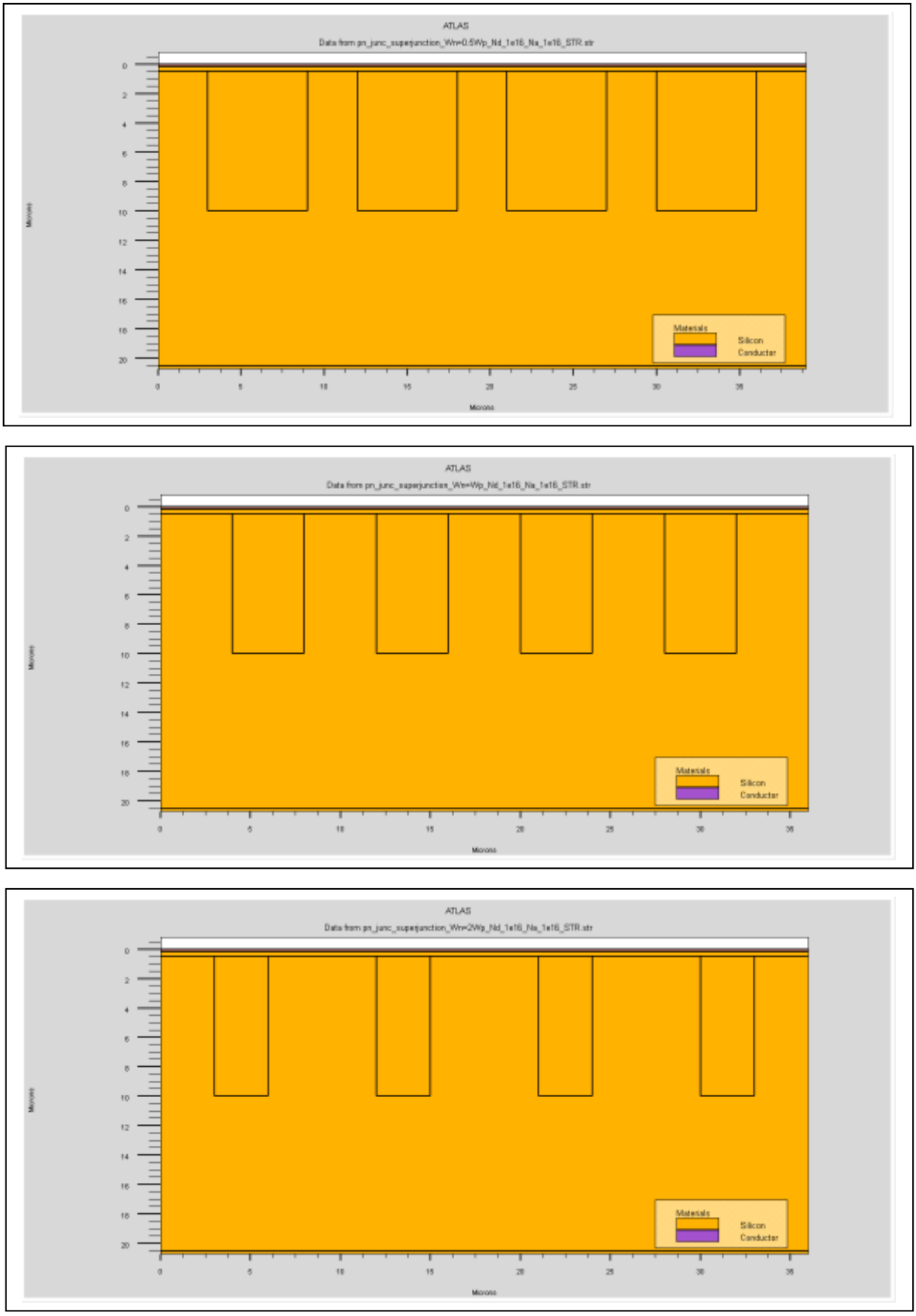


Figure3.10 *Width variation in SJ, for (Wn=0.5Wp), (Wn=Wp), (Wn=2Wp).*

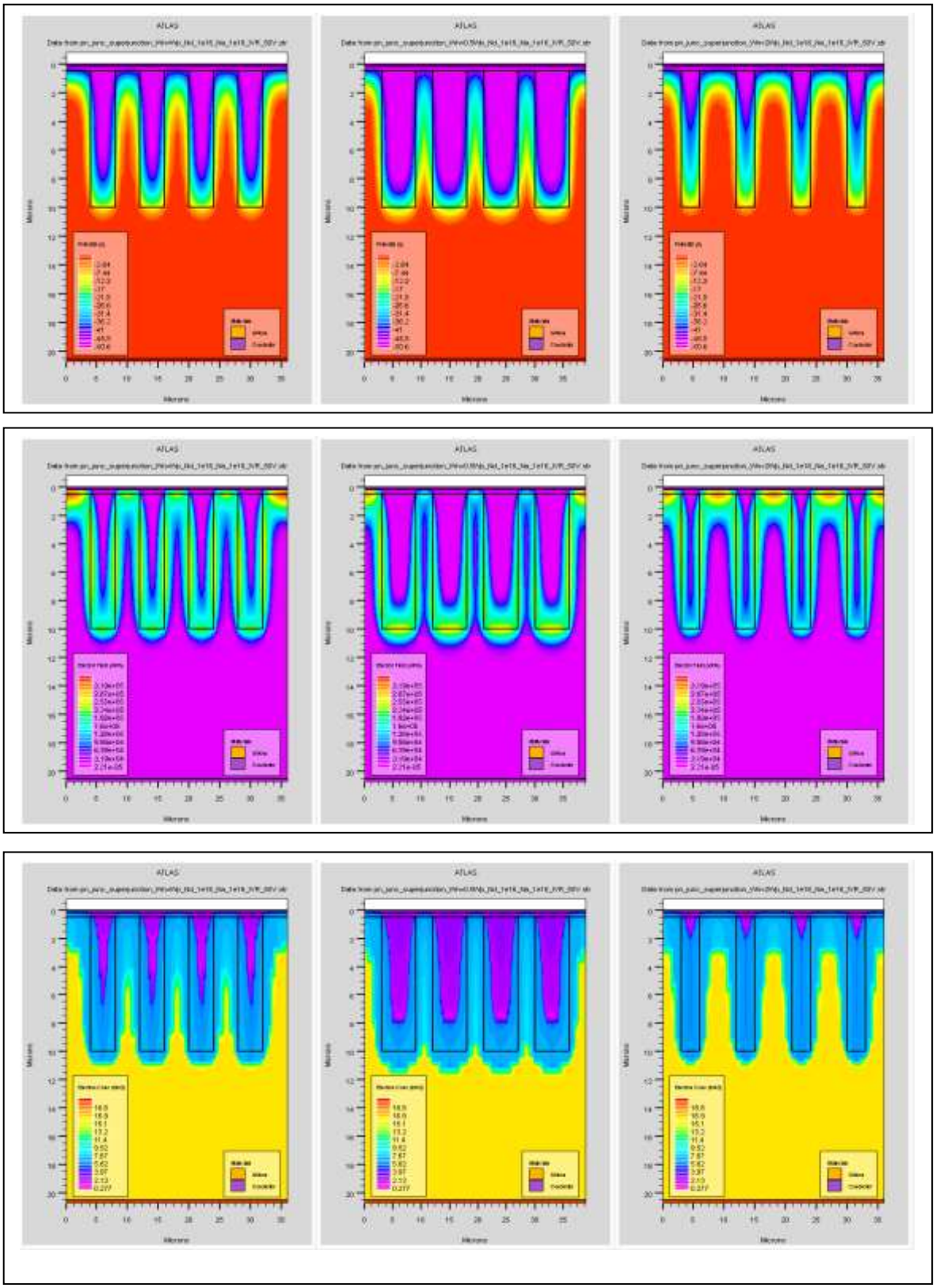


Figure3.11 *Comparison between the electric potential, the electric field and the electron's concentration for width variation in Sj reversed biased at 50 V.*

The figure 3.12 shows the variation of current (I) as a function of the voltage (V), we notice that the voltage increases in absolute value relatively when the current increases as well. Until it reaches the BV , and for it , each width has its own BV.

The results simulated by the ATLAS tool are logarithmic, it's obvious that for Wn=Wp we have the optimum width.

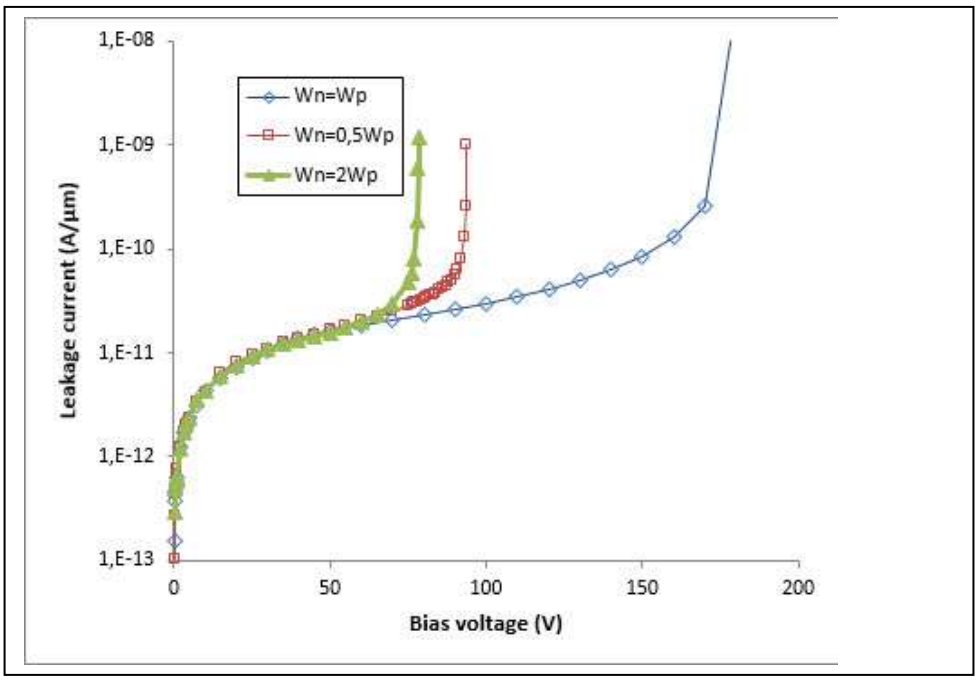


Figure3.12 *Characteristic I-V relating to the different junction width.*

b Depth variation

The figure 3.13 shows the variation in depth for an optimum width chosen in the previous simulation. As we can see in figure 3.13, that varying in depth didn't have any effect on the device performance as the graphs shows the same IV for different H length.

however this raise the question weather is depth is proportional with the doping level. further testing are ahead of us concerning the doping levels .

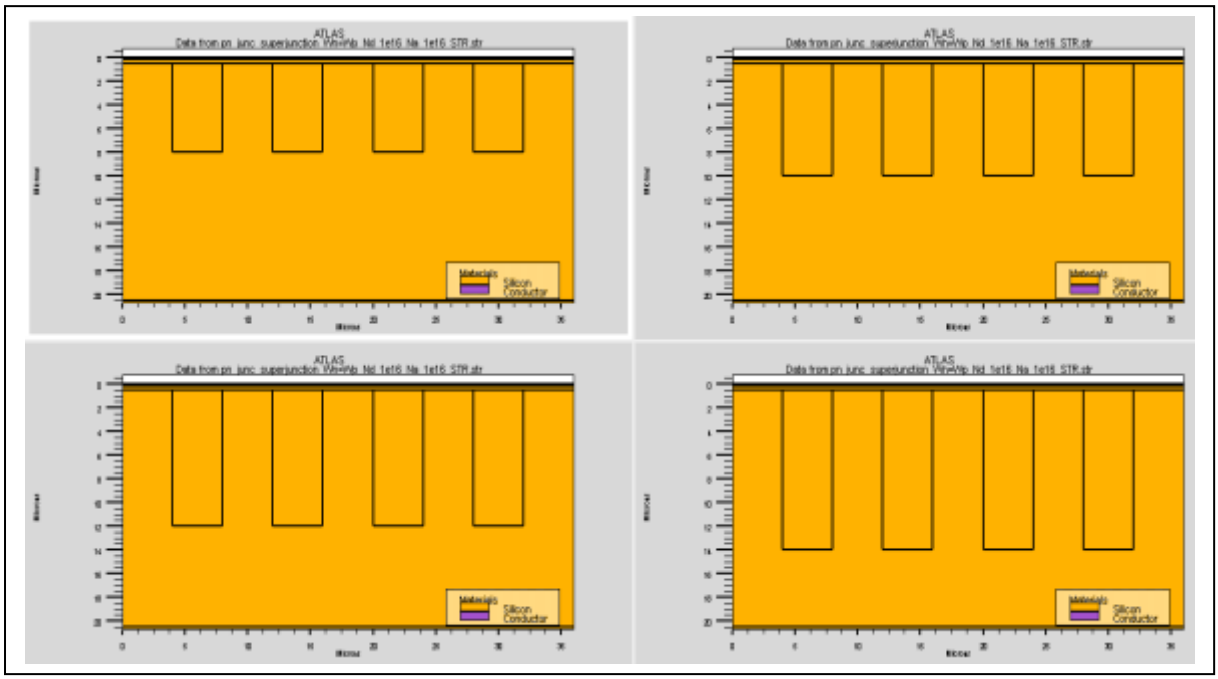


Figure3.13 *Depth variation for: (H=8) ,(H=10),(H=12),(H=14) .*

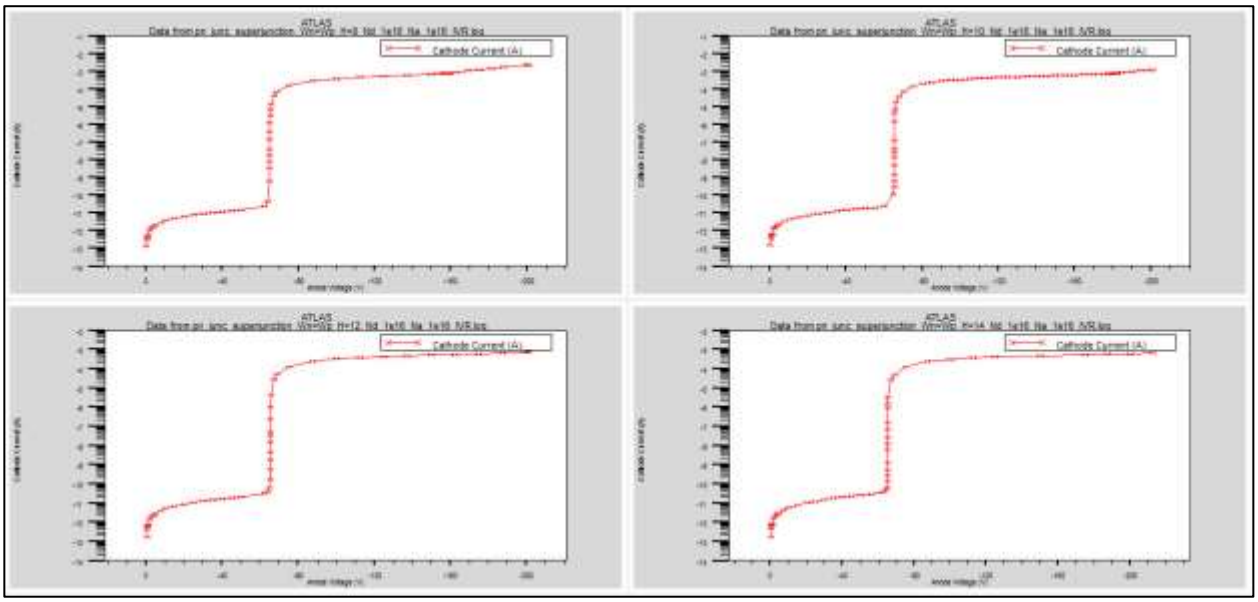


Figure3.14 IV for H variation.

3.2.5 *Technological optimization*

a Doping variation

The effect of the ion implantation dose was also simulated. This effect is pronounced on the electrical characteristics in reverse. The results on table 3.3 were accomplished by setting Nd to a fix value while varying the Na doping level, taking notice of the BV each time. It clearly shows that the devise performance is on it's best when applying lowest doping of Nd, for Nd= 2e15 : the optimum Na doping was set on 4e15 which gives a BV of a value around 300 V.

Na / Nd	2e15	4e15	8e15	2e16
2e15	250V	300V	230V	X
4e15	130V	165V	200V	100V
8e15	68V	71V	80V	85V
2e16	38V	38V	38V	40V

Table3.3 *BV for different values of Nd et Na.*

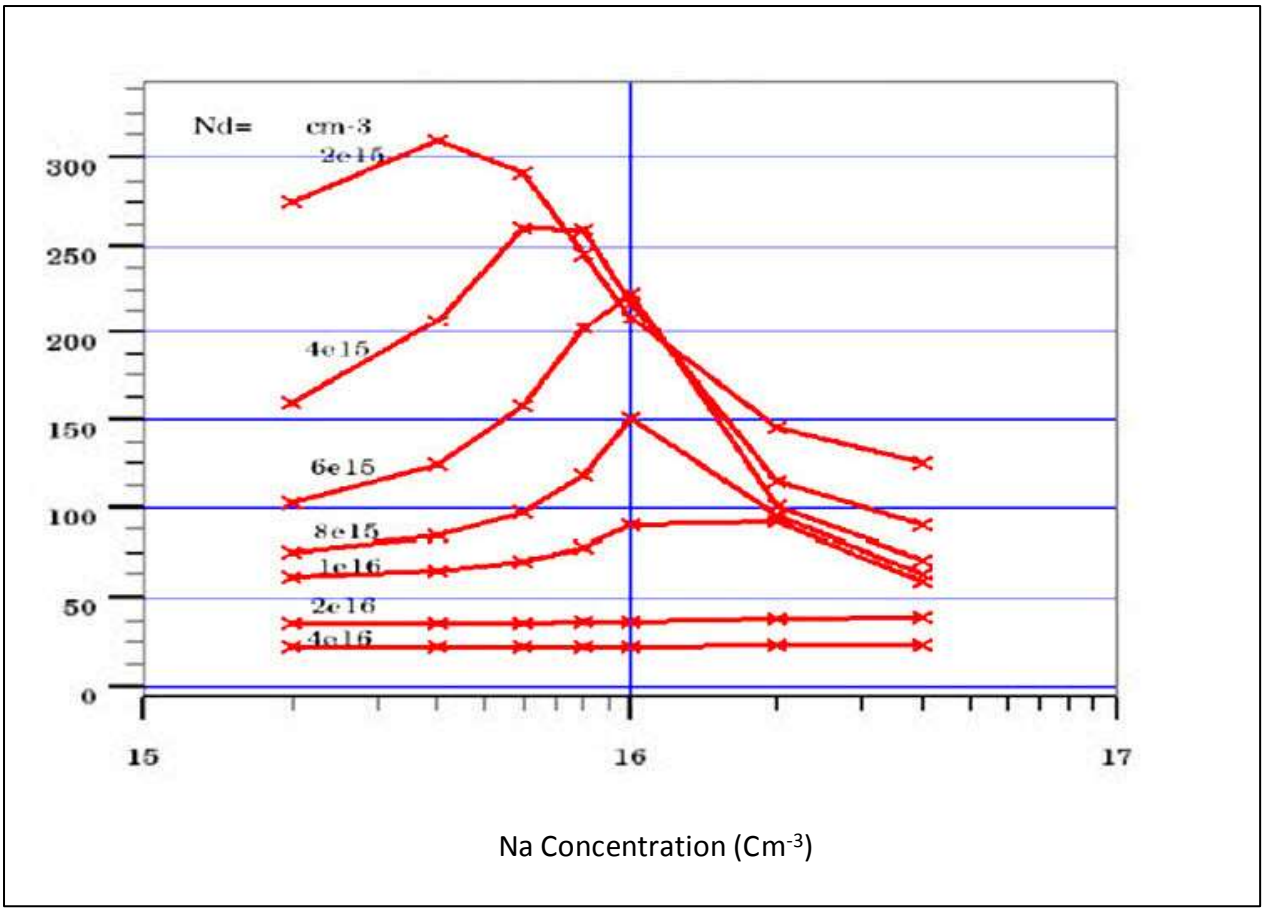


Figure3.15 *Breakdown Voltage versus Nd and Na concentration. Maximum BV Depends on the Na and the Nd ration (Na/Nd)*

The figure above illustrate that the BV depends on the ratio of the donor and that of the acceptor's concentration. This ratio is an important parameter adding to the previous ones we simulated on, all in the good of obtaining best performance results using a Super Junction technique.

General conclusion

The work done in this thesis deals with the performance of a super junction diode. the aim of this study is to increase these performances, especially the breakdown voltage.

The study will be based on the simulation of features of the powerful technology software super junction, TCAD simulator developed by the Silvaco group which is component modeling simulator capable used in continuous, transient, frequency regime. The simulation of characteristics current-voltage we use these software makes it possible to know the super junction structure performances.

First, we determine the positioning optimization as well as for the doping of the super junction structure for a high breakdown voltage possible. Secondly we applied a series of depth, width and doping for different values, in order to obtain the best results it was necessary to start the simulation with varying the width at first, and with the optimum width the depth next, which leaves the doping for last, for taking in consideration for each simulated parameters , fixing the two others .

A Super Junction structure was designed to get higher BV using ATLAS. This Super Junction has been reported with several process methods. Simple PiN and trench type p n junction diodes were compared with the Super Junction diode. The acceptor and donor concentration levels of the drift regions are very important in obtaining the highest Breakdown Voltage.

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