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Realization of a simulation interface prototype for wireless systems for SDR (Software Defined Radio)

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Thanks

As a preamble, we thank ALLAH who has helped us and given us patience and courage throughout our years of study.

We would like to sincerely thank our promoter Mr. AITSAADI HOCINE, headmaster of the electronics department, for his listening and his availability throughout the realization of this end of studies project work. He is also thanked for the inspiration, the help and the time he was kind enough to devote to us and that without him this memoir would never have seen the light of day.

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Our high regard goes to all the teachers in our department for the monumental effort they put into making us who we are now.

We do not forget our dear parents for their contribution, their support and above all their patience.

Finally, our warmest thanks go to the people who provided assistance and contributed to the development of this dissertation, as well as to the success of this wonderful academic year.

Dedication

I dedicate this modest work:

To my dearest mother,

who supported and encouraged me during these years of study;

To my very dear father,

who owes my life, my success and all my respect I hope this work reflects my gratitude and affection;

To my brothers and my sister,

who shared with me all the moments of emotion while carrying out this work;

To my partner,

for her moral support, her patience and its understanding throughout this project;

To all my best and true friends, each with their own name;

To all those I love, and to all those who are dear to me, I dedicate this work ...

Amina

Dedication

Life is an accumulation of experiences, good and bad, and today I am about to complete a new chapter in my humble life;

I am grateful to Allah for giving me the power and patience to stand here and say that I am on the verge of making the dream of a lifetime come true;

To My father,

how can words describe a galaxy ... you gave me life, courage and love, you were and you are my reason to continue;

My mother,

the one who believed in me even when I didn't, how can a princess be without a queen, I really am a version of you and I can't be more honored;

To my Sun,

you are the golden hour of a lifetime, to Chames El Assil;

To El Doctoura,

.. you are my full moon in a dark night, to Nesrine;

To my doctor,

you are the beauty in everything that ever existed, to Aya;

To my sweet baby,

you are a whole different story ... you taught me what a strong woman would look like ... but you will always be my little baby no matter how old you are ...to Soundous;

To My sixth sister,

you made me a better new version of me and i can say everything except how pure and beautiful you are, to Romaissa;

To the star of our life,

To the second version oh my hero, to my brother, no words will ever be enough to express my pride in you, to DhiaaEdine;

To my partner,

To the one I spent with my last 5 years ...the one i cried and laughed with, to Amina;

To all my teachers since i was 6;

To Blida ... To Tipaza ...

Thank you all for everything;

I love you and I dedicate this work to you;

Djihane

List of acronyms and abbreviations

ADC: Analog-To-Digital Converter.

ALU: Arithmetic and Logic Unit.

ASIC: Specific Integrated Circuit.

ASK: Amplitude Shift Keying.

BPF: Band-Pass Filters.

BPSK: Binary Phase Shift Keying.

CMOS: Complementary Metal–Oxide–Semiconductor.

CP: Cyclic Prefix.

CUDA: Compute Unified Device Architecture.

DAC: Digital-To-Analog Converter.

DDC: Digital Down Converter.

DFT: Discrete Fourier Transform.

DFT: Discrete Fourier Transform.

DPSK: Differential Phase Shift Keying.

DSBSC: Double-Sideband Suppressed Carrier.

DSP: Digital Signal Processor.

DTH: Direct-To-Home.

DUC: Digital Up-Converter.

DVT: Digital Video Broadcasting.

EM: electromagnetic.

FDD: Frequency Division Duplex.

FDM: Frequency Division Multiplexing.

FFT: Fast Fourier Transform.

FFT: Fast Fourier Transform.

FIR: First Information Report.

FLOPS: Floating Point Operations Per Second.

FPGA: Field Programmable Gate Array.

FSK: Frequency Shift Keying.

GNSS: Global Navigation Satellite System.

GOPS: Giga Operations Per Second.

GPP: General-Purpose Processor.

GPU: Graphical Processing Units.

GUI: Graphical User Interface.

HLS: High-Level Synthesis.

HPC: High-Performance Computing.

ICI: Inter-Carrier Interference.

IDFT: Inverse Discrete Fourier Transform.

IEEE: Electrical and Electronics Engineers.

IF: Intermediate Frequency.

IFFT: Inverse FFT.

LDPC: Low-Density Parity Check.

LNA: Low Noise Amplifier.

LOS: Line of Sight.

LOS: Line-Of-Sight.

LPF: low-pass filter.

LUT: look-up tables.

MAC: Multiplication And Accumulation.

MIMO: Multiple-Input and Multiple-Output

NFV: Network Function Virtualization

NLOS: No line of sight.

NRZI: Non Return to Zero Inverted.

OFDM: Orthogonal Frequency Division Multiplexing.

PAM: Pulse Amplitude Modulation.

PL: Path Loss.

PPL: Phase Locked Loop.

QAM: Quadrature Amplitude Modulation.

QPSK: Quadrature Phase Shift Keying.

RF: Radio frequency.

RFFE: Radio Frequency Front End.

RFID: Radio-Frequency Identification.

RTL: Register Transfer Level.

SDR: Software-Defined Radio.

SFDR: Spurious-Free Dynamic Range.

SNR: Signal-to-Noise Ratio.

SRC: Sampling Rate Conversion.

TDD: Time Division Duplex.

VHDL: VHSIC Hardware Description Language.

WiMAX: Worldwide Interoperability for Microwave Access.

WLAN: Wireless Local Area Network.

x-DSL: x Digital Subscriber Line.

ملخص :معايير الاتصالات اللاسلكية تتغير باستمرار وتتطور بسرعة. يشكل هذا تحديًا للباحثين والمصنعين ، الذين يجب أن يتكيفوا معه في عملهم. أدت الحاجة إلى طريقة وأجهزة للتعامل مع هذا التغيير المستمر إلى تعميم استخدام ومفاهيم النماذج الأولية السريعة ومنصات البرامج الراديوية القائمة على .(SDR) FPGA من الواضح أن بعض الأساليب والأدوات القائمة على هذا المفهوم ظهرت في برمجة برامج الراديو. وتتمثل خصائص كل هذه الأساليب في قدرتها على توفير وقت التطوير وسهولة تطبيقها. لم تعد الأدوات المقدمة تتطلب معرفة متعمقة بلغات برمجة الأجهزة أو الأجهزة المستهدفة. العمل الموصوف في هذه الأطروحة هو تطبيق أسلوب النموذج الأولي على منصة SDR (USRP).لا تتطلب هذه الطريقة أي أسطر من التعليمات البرمجية لأنها تستند إلى.MATLAB / Simulink

تُســتخدم أدوات البرامج هذه لإنشــاء بنية المقدّر ، والتي يتم تحويلها بعد ذلك إلى لغة أجهزة (HDL) وتنفيذها على النظام الأساسي (USRP) SDR الهدف .

Abstract: Wireless telecommunications standards are constantly changing and evolving rapidly. This poses a challenge for researchers and manufacturers, who must adapt to it in their work. The need for a method and hardware to cope with this constant change has popularized the use and concepts of rapid prototyping and FPGA-based software radio (SDR) platforms. Obviously, some methods and tools based on this concept have appeared in the programming of software radio. The characteristics of all these methods are that they can save development time and are easy to apply. The provided tools no longer require in-depth knowledge of hardware programming languages or target hardware. The work described in this thesis is the application of the prototype method on the SDR platform (USRP). This method does not require any lines of code because it is based on MATLAB/Simulink.

These software tools are used to create the estimator architecture, which is then converted into a hardware language (HDL) and implemented on the target SDR (USRP) platform.

Résumé : Les normes de télécommunications sans fil changent constamment et évoluent rapidement. Cela représente un défi pour les chercheurs et les industriels, qui doivent s'y adapter dans leur travail. Le besoin d'une méthode et d'un matériel pour faire face à ce

changement constant a popularisé l'utilisation et les concepts de prototypage rapide et de plates-formes de radio logicielle (SDR) basées sur FPGA. Evidemment, certaines méthodes et outils basés sur ce concept sont apparus dans la programmation de logiciels radio. Les caractéristiques de toutes ces méthodes sont qu'elles permettent de gagner du temps de développement et sont faciles à appliquer. Les outils fournis ne nécessitent plus une connaissance approfondie des langages de programmation matérielle ou du matériel cible. Le travail décrit dans cette thèse est l'application de la méthode prototype sur la plateforme SDR (USRP). Cette méthode ne nécessite aucune ligne de code car elle est basée sur Matlab/Simulink.

Ces outils logiciels sont utilisés pour créer l'architecture de l'estimateur, qui est ensuite convertie en un langage matériel (HDL) et implémentée sur la plate-forme SDR cible (USRP).

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General Introduction

Various forms of communication have evolved over the millennia. The spoken word can be transmitted from one person, and heard or received by another. In modern times town criers hold an annual contest to discover who can shout a comprehensible message over the greatest distance.

However, while the world record is for loudest crier is 112.8 decibels, it can only be understood at less than 100 meters. The desire to communicate more effectively than shouting, is old as speech itself. With modern advances in computing technologies, digital signal processing and digital communication algorithms, artificial intelligence, radio frequency (RF) hardware design, networking topologies, and many other elements have evolved modern communication systems into complex, intelligent, high-performance platforms that can adapt to operational environments and deliver large amounts of information in real-time, error-free. The latest step in communication systems technology is the software-defined radio, or SDR, which adopts the most recent advances in all fields to yield the ultimate transmitter and receiver.

The need for affordable and efficient means to test new and improved transmission methods is endless. Due to the high cost of RF equipment and the limitations imposed by fixed parameter hardware, the idea of a highly dynamic system for testing new methods is seen as highly desirable.

Nowadays and thanks to SDR technologies the realization of transmission chains becomes easy accessible.

our goal through this memory is to exploit the SDR technology and to enter the world of rapid prototyping thanks to the hard soft compatibility offered by this future-oriented equipment and to show how reliable and efficient it is.

we are eager to test SDR prototyping techniques, we will present to you the main types and components of SDR, then we will detail everything about the transmission chains and the types of modulations,

finally, we will use the USRP cards under several types of modulations to see their performance.

SDR is a very broad technology it contains many models and types

in this thsis, we will go into the heart of one of the most common SDR cards, the USRP 2920.

the first chapter will bring together all the definitions and concepts of SDR components starting of rf antennas, processors and their main qualities.

we will also see all the software options to better communicate with the cards (GNU radio, MATLAB etc ...).

the second chapter will touch on everything that goes into making a digital transmission chain, the types of digital modulation, we will discuss the propagation in the wireless channel and finally the OFDM modulation.

in the last chapter we will use USRP boards to implement three different types of modulation and observe the signal state and how it behaves

CHAPITRE I

Introduction to the SDR and USRP's technologies

1. Introduction to the Software-Defined Radio

Radio is a system with technology for wireless transmission of information through electromagnetic radiation. In the past, radios consisted of many discrete circuits and electronic devices, which had fixed functions and could not be modified after manufacture. For example, using a traditional radio cannot convert a commercial FM receiver into a digital radio receiver. However, now with software-defined radio (SDR), people can buy a USB DVB-T2 dongle to receive terrestrial TV in a computer and use it as a GPS receiver, or to decode ADS-B (Automatically Dependent Surveillance Broadcast) Signal and get the position of all nearby planes. This shows how SDR is superior to traditional radios in terms of flexibility and reconfigurability.[22]

Many definitions can be found to describe software-defined radio, also known as Software defined radio or SDR. SDR Forum, in cooperation with the Institute of Electrical Engineering and Electronic Engineers (IEEE) P1900.1 group, working to establish the definition of SDR This provides a consistent and clear overview of the technology and its related benefits. Simply put, software-defined radio is defined as 1: "Radio in which part or all of the physical layer functions are defined by software". [23]

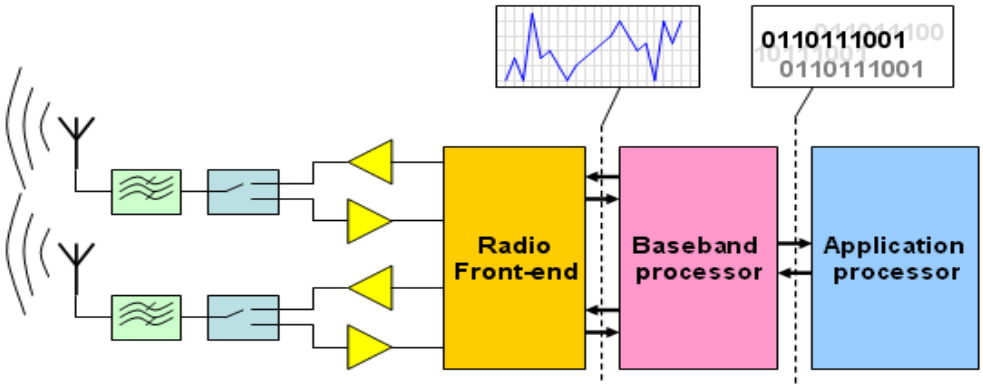

Figure1. 1:Software-defined radio

2. Concepts and architecture

In this section, we will study the general architecture of SDRs, their main components, and their processing requirements. As mentioned in the previous section, SDR plays a vital role in the development of wireless standards due to its flexibility and programmability. This is because most digital signal processing and digital front ends (including channel selection and modulation/demodulation) occur in the digital domain.

This is usually performed in software running on a processor, such as GPP and DSP. However, it can also run-on programmable hardware (i.e., FPGA).

Generally speaking, from the perspective of the transmitter, it is necessary to generate the baseband waveform first, then the intermediate frequency (IF) waveform, generate the radio frequency waveform, and then send it through the antenna. From the receiver's perspective, this RF signal is sampled and demodulated, and then decoded.

In order to provide more details of the process, we study the receiving end of the system as follows. The RF signal from the antenna is amplified, and the tuned RF stage can amplify a certain range of frequency bands. This amplified radio frequency signal is then converted into an analog intermediate frequency signal. An analog-to-digital converter (ADC) digitizes this IF signal into digital samples. Then, it is sent to the mixer stage. The mixer has another input from the local oscillator, the frequency of which is set by the tuning control.

The mixer then converts the input signal to baseband. The next stage is essentially an FIR filter that allows only one signal. This filter limits the signal bandwidth and acts as a decimation low-pass filter. The digital down converter includes a large number of multipliers, adders and shift registers in the hardware to complete the above tasks.

Next, the signal processing stage performs tasks such as demodulation and decoding. This stage is usually handled by dedicated hardware (such as an application specific integrated circuit (ASIC)) or other programmable alternatives (such as FPGA or DSP). As shown in Figure 1 (a) and (b), at a higher level, a typical SDR transceiver includes the following components: signal processing, digital front-end, analog RF front-end, and antenna. [4]

A. Antenna

SDR platforms usually use multiple antennas to cover a wide range of frequency bands. Antennas are often called "smart" or "smart" because they can select frequency bands and adapt to mobile tracking or interference cancellation. In the case of SDR, antennas need to meet a specific list of requirements, such as self-adaptive (that is, flexibly tuned to Multiple frequency bands), self-alignment (i.e., beamforming capability) and self-healing (i.e., interference suppression). [4]

B. RF Front End

This is a radio frequency circuit whose main function is to send and receive signals at various operating frequencies. Its other function is to change the signal to intermediate frequency (IF)/slave intermediate frequency (IF). The operation process is divided into two types, depending on the direction of the signal (i.e., Tx or Rx mode):

- In the transmission path, a digital-to-analog converter (DAC) converts digital samples into analog signals, which are then fed to the RF front-end.
  This analog signal is mixed with a preset radio frequency, modulated, and then transmitted.

- In the receiving path, the antenna captures radio frequency signals. The antenna input uses a matching circuit to connect to the RF front end to ensure the best signal power transmission. It then passes through a low noise amplifier (LNA) close to the antenna to amplify weak signals and minimize noise levels. This amplified signal is fed into the mixer along with the signal from the local oscillator (LO) to down-convert it to IF. [4]

C. Analogy-to-Digital and Digital-to-Analogy Conversion

As mentioned in the previous section, the DAC is responsible for generating the analog signal to be transmitted from the digital samples. On the receiver side, the ADC is located in the radio receiver and is an essential component. The ADC is responsible for converting

continuous-time signals into discrete-time binary coded signals. ADC performance can be described by various parameters, including:

(i) Signal-to-Noise Ratio (SNR): he ratio of signal power to noise power in the output, (ii) resolution: number of bits per sample, (iii) spurious-free dynamic range (SFDR): Carrier signal to the next strongest noise component or spur, and (iv) power consumption. Advances in SDR development have provided impetus for the improvement of ADC performance. For example, because the power consumption of the ADC affects the life of the battery-powered SDR, more energy-efficient ADCs have been developed. [4]

D. Digital Front End

The digital front end has two main functions [4]:

- Sampling rate conversion (SRC), which is a function to convert samples from one rate to another. This is necessary because the two communicating parties must be synchronized.

- Channelization, including up/down conversion at the transmitter and receiver respectively. It also includes channel filtering, where channels divided by frequency are extracted.

  Examples include interpolation and low-pass filters, as shown in Figure 1.2. In the SDR transceiver, the following tasks are performed in the digital front end:

- At the transmitting end (Figure 1.2 (a)), a digital up-converter (DUC) converts the above-mentioned baseband signal to IF. The DAC connected to the DUC then converts the digital IF samples into analog IF signals. Then, the RF upconverter converts the analog IF signal to RF frequency.

- At the receiving end (Figure 1.2(b)), the ADC converts the IF signal into digital samples. These samples are then sent to the next module, the digital down converter (DDC). DDC includes a digital mixer and a numerically controlled oscillator. DDC extracts the baseband digital signal from the ADC, and after processing by the digital front-end,

forwards the digital baseband signal to the high-speed digital signal processing module.[4]

E. Signal Processing

Signal processing operations such as encoding/decoding, interleaving/de-interleaving, modulation/demodulation, and scrambling/descrambling are performed in this block. The coding of the channel is used as an error correction code. Specifically, the encoded signal includes redundancy, and the receiver's decoder uses the redundancy to reconstruct the original signal from the damaged received signal. Examples of error correction codes include convolutional codes, turbo codes, and low-density parity check (LDPC). Due to the data transmission and storage scheme, the decoder constitutes the most computationally intensive part of the signal processing block. The second part considered to be very complex and expensive (in terms of area and power) is the Fast Fourier Transform (FFT) and Inverse FFT (IFFT) as part of the modulation stage. [4]

The signal processing block is usually called the baseband processing block. When discussing SDR, the baseband module is the core of the discussion, because it constitutes most of the digital domain of the implementation. This implementation runs on hardware circuits that can effectively process signals. Examples include ASIC, FPGA, DSP, GPP, and GPU. The second part of the implementation is software, which provides functions and high-level abstractions to perform signal processing operations. In the next section, we will examine the above hardware platforms and analyze various design methods in detail. [4]

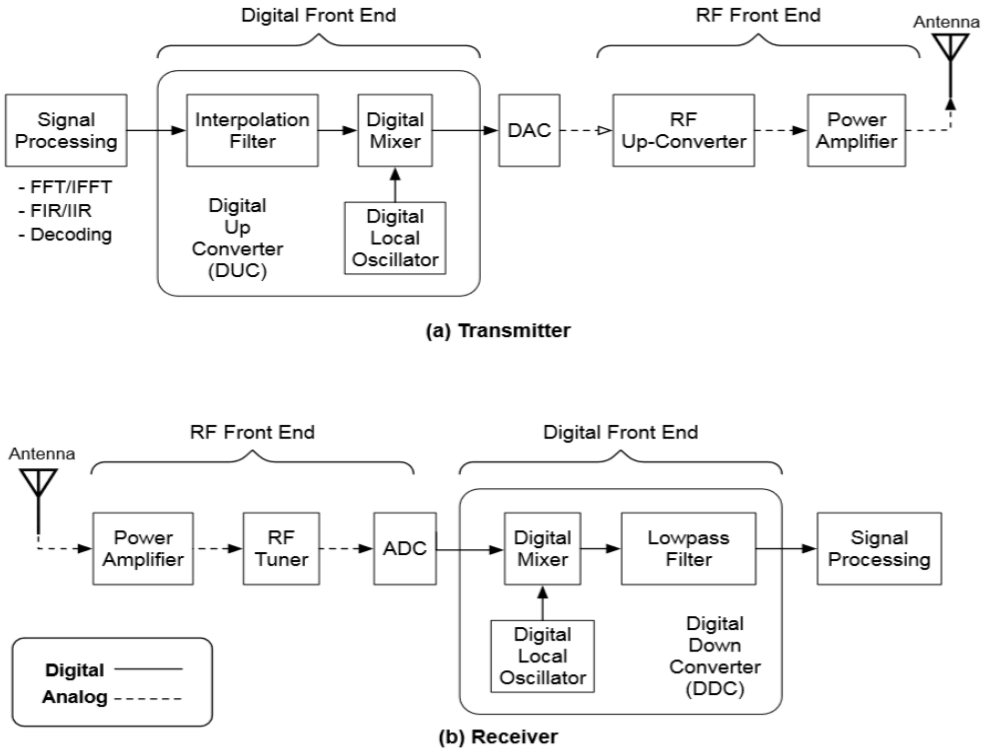

Figure1. 2:SDR architecture. Sub-figure (a) shows SDR from a receiver's point of view, and sub-figure (b) shows SDR from a transmitter's point of view

3. Design Approaches

In this section, we discuss the classification of various SDR design methods for baseband processing blocks, namely GPP, GPU, DSP, FPGA, and methods based on co-design. In this classification, we analyze and compare SDR platforms based on a set of performance indicators in the standards we introduced. The standard includes [4]:

- Flexibility and reconfigurability. Modulation and air interface algorithm and protocol development capabilities, only need to load new software onto the platform
- Adaptability. The SDR platform can adjust its functions as the network or traffic operation requirements change.
- Calculate ability. The processing rate of the SDR platform is Giga Operations per second (GOPS).

- Energy efficiency. Total power consumption (usually within a few hundred milliwatts), especially for mobile and IoT deployments. [4]
- Cost. The total cost of the SDR platform, including time to market, development and hardware costs. [4]

A. GPP-based

The first way to implement the SDR platform is to use a general-purpose processor (GPP), or well-known general-purpose computer microprocessor, such as x86/64 and ARM architecture. Examples of SDR platforms that use GPP include Sora, KUAR, and USRP.[4]

a. Definition and use:

GPP is a clock-driven and register-based digital circuit that can handle different functions and operate on the data stream expressed in binary.

These GPPs can be used for a variety of purposes, making them ideal for an unlimited number of applications, eliminating the need to build application-specific circuits, thereby reducing the overall cost of running applications. [4]

GPP is usually the preferred hardware platform for academic researchers because of their flexibility, richness, and programmability, which is one of the main requirements of the SDR platform.

In addition, compared with DSP and FPGA, researchers prefer GPP because they are more familiar with GPP and its software framework. From a performance point of view, GPP is rapidly increasing, not only due to technological advancements in CMOS technology, but also due to the increase in the average number of instructions processed per clock cycle. The latter is achieved in different ways, especially using parallelism within and between processors. This led to the development of multi-core GPP. [4]

b. Adoption and GPU:

Architecturally, GPP's instruction set includes instructions for different operations, such as arithmetic and logic unit (ALU), data transfer, and I/O. GPP processes these commands

in order. Due to sequential processing, GPP is not convenient for high-throughput calculations with real-time requirements (i.e., high throughput and low latency).

For example, using GNU Radio to implement the IEEE 802.11 standard (which requires a 20MHz sampling rate) will be challenging because GNU Radio is limited by the limited processing power of GPP. This will cause the GPP core (of the connected PC) to reach saturation, and the frame will be corrupted and discarded. In addition, wireless protocols require predictable performance to ensure that timing constraints are met.

However, the conditional branch instructions in the GPP instruction set can cause out-of-order execution, which makes it infeasible to achieve predictability. [4]

B. DSP-based

DSP-based solutions can be considered as special cases of GPP-based solutions, but due to its popularity and unique processing characteristics, it is worth discussing separately. An example of DSP-based SDR is the Atomix platform using TI TMS320C6670 DSP [4].

a. Definition and use:

DSP is a special type of microprocessor, optimized to process digital signals. In order to help understand the difference between DSP and GPP, we should first notice that both can implement and handle complex arithmetic tasks.

Tasks such as modulation/demodulation, filtering, and encoding/decoding are usually and often used in applications such as speech recognition and image processing., And communication system.

However, because the DSP architecture (for example, RISC-like architecture, parallel processing) is specifically optimized for arithmetic operations (especially multiplication), they can be implemented faster and more efficiently. Because DSPs can provide high performance with lower power consumption, they are more suitable for deploying SDRs than GPPs. The DSP examples specially designed for the SDR platform are TI TMS320C6657 and TMS320C6655.

These DSPs are equipped with hardware accelerators for complex functions, such as Viterbi and Turbo decoders.

b. Adoption:

As mentioned in the previous section, GPP provides average performance for a wide range of applications. Needless to say, this level of performance may be sufficient for research and academia, but if the system is to be commercially deployed, certain performance requirements must be met. For this reason, compared with GPP, DSP is tailor-made for effective processing of digital signals, using functions such as combined multiplication and accumulation (MAC unit) and parallelism. DSP manufacturers usually sell these products in two ways: optimizing performance and optimizing energy. Therefore, when used for SDR, high-performance and energy-efficient products can be used for BS and edge devices, respectively. [4]

C. FPGA-based

Another way to implement SDR is to use programmable hardware, such as FPGAs. An example of an FPGA-based SDR platform is Airblue, based on Xilinx Zynq's IEEE 802.11ah implementation, which uses the same FPGA board to implement a complete communication system with channel coding. [4]

a. Definition and use:

FPGA is a group of programmable logic blocks, such as general logic, memory and multiplier blocks, which are surrounded by wiring structures, which are also programmable.

The circuit has the ability to implement any design or function and is easy to update. Although FPGAs consume more power and occupy more area than ASICs, the programmable features are the reason for their increasing adoption in a wide range of applications. In addition, when the reconfiguration delay is in the millisecond level, SDR can seamlessly switch between different modes and protocols.

Another major difference is that ASICs are expensive to manufacture (at least tens of thousands of dollars) and take several months, while FPGAs can be reprogrammed quickly, and the cost is between tens to thousands of dollars, at most. Compared with processors such as GPP and DSP, low-end product cycles and attractive hardware

processing advantages (such as high-speed performance, low power consumption, and portability) make FPGAs a contender that offers the best of both worlds. [4]

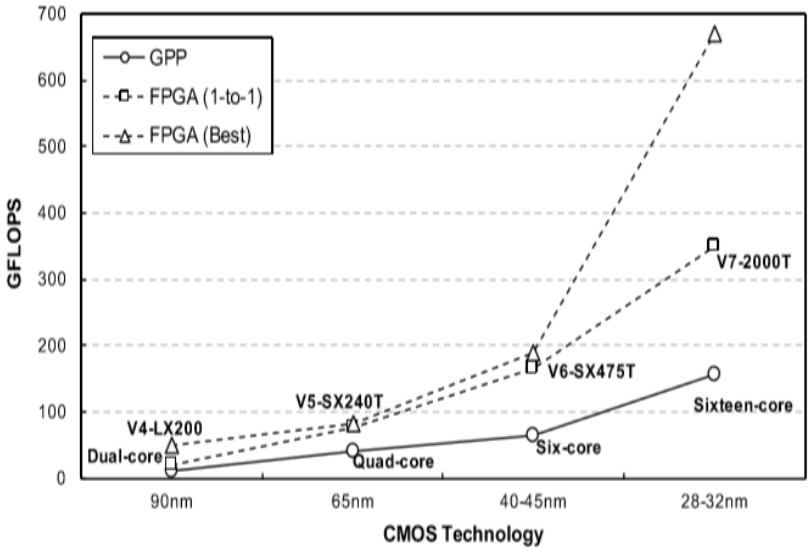

Figure1. 3:Peak performance of GPPs versus FPGAs when performing 64-bit floating point operations

b. Adoption:

In the past ten years, FPGAs have significantly improved and become more computationally powerful, and now exist in many different versions, such as Xilinx KintexUltraScale and Intel Arria 10.

In addition, the availability of various tool sets makes FPGAs more accessible, which provides them with advantages. This is due to the availability of compilers that can generate register transfer level (RTL) code from high-level programming languages, such as Verilog and VHDL, which need to run on the FPGA. This process is commonly referred to as high-level synthesis (HLS). Examples of such compilers include HDL Coder for MATLAB code and Xilinx HLS or Altera Nios II C2H compilers for C, C++, and System C. HLS allows software engineers to use familiar programming languages to design and implement applications on FPGAs, such as SDR code, namely C, C++, System C, and

MATLAB, without the need for a priori rich knowledge of the target hardware architecture.

These compilers can also be used to speed up or speed up part of the software code running on GPP or DSP, which can slow down or frustrate overall performance. In addition, FPGAs can achieve high performance while still consuming less energy than the previously discussed processors (for example, Intel Stratix 10 FPGAs can achieve up to 100 GFLOPS/W, while NVIDIA GeForce GTX 980 Ti can achieve 23 GFLOPS/W. In addition, Power consumption can be further reduced through the implementation of multiple technologies. These techniques can be at the system, device, and/or architecture level, such as clock gating and glitch reduction. Table I summarizes the widely used FPGA platforms.[4]

	FPGA only			**SoC**		
	Xilinx Kintex-7(XC7K70T)	**Intel Cyclone V GX (C5)**	**Lattice ECP3-70EA)**	**Xilinx Zynq-700(Z-7020 XC7Z020)**	**Intel Cyclone V SE SoC(A5)**	**Micro semi SmartFuion2(M2S090)**
Logic Cells(K)	65.6	77	67	85	85	86.31
Memory (Mb)	4.86	4.46	4.42	4.9	3.97	4.488
DSP Slices	240	150	128	220	87	84
Cost (USD)	130	185	80	110	110	155
Soft Core	N/A	N/A	N/A	Dual-core ARM Cortex-A9	Dual-core ARM Cortex-A9	ARM Cortex-M3

Table1. 1:Comparison of FPGAs and FPGA-based SoCs

D. Hybrid Design (a.k.a., co-design)

The fourth way to implement SDR is a hybrid approach, combining hardware and software-based technologies into one platform. This is often referred to as a collaborative design or hybrid approach. Examples of SDRs that use co-design methods include WARP and CODIPHY. [4]

a. Definition:

Hardware/software co-design has existed as a concept for more than a decade, and it has developed at a faster rate in the past few years because people are increasingly interested in new and different methods to solve integrated circuit design problems. Even if GPP becomes more powerful than ever and adopts a multi-core design, it is obvious that in order to achieve higher performance and realize applications that require real-time processing, designers have to turn their attention to new hardware solutions. On the design scheme, namely, FPGA and ASIC. Co-design means using hardware design methods represented by FPGA architecture and software design methods represented by processors. As more and more applications (such as automobiles, communications, and medical) become more complex and larger, it has become a common practice to design systems that integrate software (such as firmware and operating systems) and hardware. In recent years, due to advances in advanced synthesis and development tools, these tools can not only generate efficient RTL from software code, but also define the interface between the two parties, which makes this feasible. The industry has realized the huge market for collaborative design and has provided various SoC boards, which include multiple processors in addition to the FPGA architecture. For example, the Xilinx Zynq board includes an FPGA structure and two ARM Cortex-A9 processors. In addition to the above advantages, there are other reasons that make co-design more interesting, including faster time to market, lower power consumption (when optimized for this), flexibility, and higher processing speed. The typical hardware system is used as the acceleration software bottleneck. [4]

b. Adoption:

SDR can be considered as an inherently hybrid or heterogeneous system, which means that hardware and software blocks are required. This is because the control part is usually processed by a general-purpose processor, while other functions, such as signal processing, are handled by a dedicated processor (such as DSP), and sometimes dedicated hardware (such as FPGA) is used for acceleration. This design method fits well with SDR and can be fully utilized to meet certain requirements related to its attractive features. For example, moving part or all of the acceleration module to the FPGA architecture helps push the processing time to the limit to achieve the real-time performance of the actual deployment.

In addition, by carefully implementing RTL optimization techniques, it is possible to develop energy-saving systems for mobile and IoT applications. On the other hand, running most of the MAC layer operations on one processor or multiple processors can facilitate easy reconfiguration. Therefore, different partitioning schemes can be adopted to meet the requirements of the application at hand. It is worth noting that due to the growing demand for such devices, FPGA vendors, namely Intel and Xilinx, are expanding their product base with more SoCs and multi-processor SoCs (MPSoCs).

An example of implementing SDR on MPSoC is. In the white paper, National Instruments (the company that owns USRP) predicts that the future of SDR is essentially a collaborative design implementation, especially with the introduction of FPGAs, which are equipped with a large number of DSP Slice is used to handle intensive signal processing tasks, as shown in Figure 2.3. This can also be seen from the USRPE310 model, which contains a Xilinx ZynqSoC. [4]

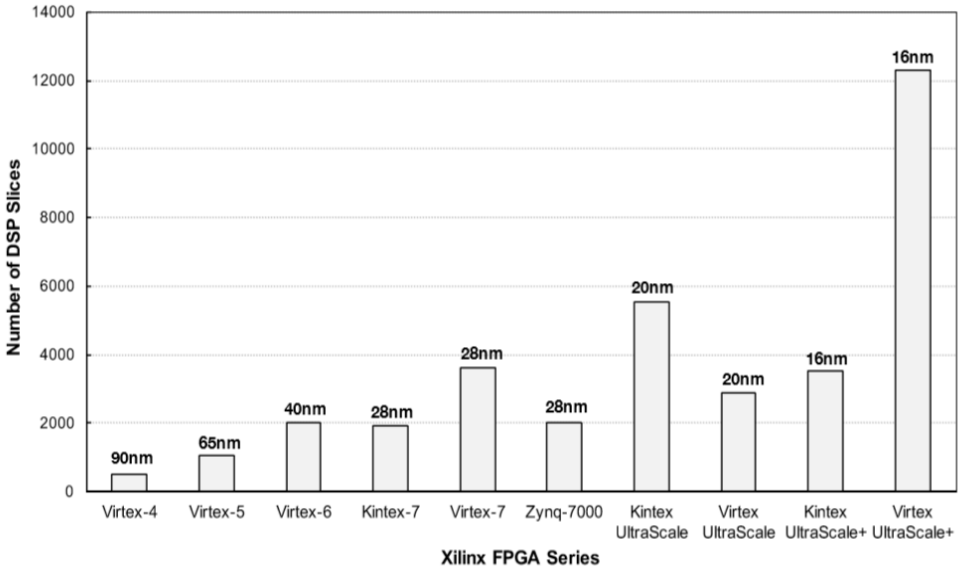

Figure1. 4:Number of DSP Slices in Xilinx FPGAs. The values on top of the bars refer to the CMOS technology used.

E. Comparison

When we choose different design methods and hardware platforms for a wide range of SDR platforms, we plan to use a cross-platform implementation of one of the wireless communication protocols to perform a one-to-one analysis and comparison. Instead, what is available in the literature is a series of abstract comparisons using a set of benchmarks for high-performance computing (HPC) rather than SDR applications. It is difficult to draw conclusions from these figures alone, because performance comparisons in the SDR field need to be tested in real life.

In Table II, we provide a high-level comparison between the three main design methods as a guide for designers to choose the method that best meets their application specifications. In this comparison, we focus on features that are important to SDR design. However, we do not make assumptions about the best approach and believe that developers are responsible for making their best judgments Depends on the application area. Note that we did not include GPUs in this table because they usually act as coprocessors for GPP, and their addition usually improves performance. We also do not include co-design because it combines GPP and FPGA. [4]

	GPP	**DSP**	**FPGA**
Computation	Fixed arithmetic engines	Fixed arithmetic engines	User configurable logic
Execution	Sequential	Partially parallel	Highly parallel
Throughput	Low	Medium	High
Data rate	Low	Medium	High
Data width	Limited by bus width	Limited by bus width	High
Programmability	Easy	Easy	Moderate
Complex algorithms	Easy	Easy	Moderate
I/o	Dedicated ports	Dedicated ports	User configurable ports
Cost	Moderate	Low	Moderate
Power efficiency	Low	Moderate	High
Form factor	Large	Medium	Small

Table1. 2:Comparison of SDR design approaches.

4. SDR's Application and operating principle

Software-defined radio (SDR) has been continuously evolving since its inception to provide communication and signal processing capabilities to meet multiple fields and needs from amateur radio to mission-critical wireless systems.

SDR transmits and receives radio data, and quickly and accurately converts between the analog domain and the digital domain on multiple frequency bands, and has functions that are implemented in software rather than hardware. [1]

SDR can be easily integrated into existing or new systems, replacing multiple individual products, and its application can be modified by changing the FPGA or through software on the host.

These modifications are to adapt to technological changes rather than obsolescence. With a powerful long-term investment product, you can share the cost over a longer period of

time, because the service life of the system is usually much longer than that of traditional pure hardware solutions.

With SDR, you only need to upgrade/repair with one supplier, compile all components in a fully integrated boxed platform, save valuable space, and provide a more simplified, user-friendly interface and front-end. [1]

One of the key components that make SDR a technological powerhouse is FPGA (Field Programmable Gate Array); this allows the system to take on new roles, receive updates, and adjust performance parameters for unique environments and conditions. In addition, the system includes signal filtering, mixing, signal amplification, modulation/demodulation, and other forms of digital signal processing (DSP) to ensure that the platform is fully utilized and meets all requirements related to different wireless applications. [1]

The following are some applications/fields of using SDR and unique overall advantages.

In low-latency applications, you can perform all necessary modulation and demodulation on the FPGA to reduce the overall system delay, and adjust the transaction between delay and reliability according to the strategy that best suits the given requirements and high-frequency conditions. [1]

For radar applications, SDR has a configurable radio front end, which allows the same platform to be used for different radar applications because it can operate on different frequency bands of the radio spectrum. For example, airport surveillance radars operate on S-band, while oceans operate on X-band. An SDR platform at a maritime airport can be used to monitor both.

The overall reduction in complexity can save space, cost, time to market and reduce supply chain barriers. Smaller, more efficient platforms allow SDRs to be installed in more environments because they are more compact and easier to use and maintain than traditional hardware-centric options.

In GNSS applications, SDR can receive signals of various frequencies from multiple satellite constellations, which means that a single device can access different navigation systems and can be updated to connect to new satellites launched in the future. [1]

5. SDRs software

In this section, we will review the existing software tools used for SDR development. For each design method, we discuss compatible development tools and list their functions. [4]

A. MATLAB and Simulink

MATLAB is widely used in all fields of applied mathematics, university education and research, and industry. MATLAB stands for Matrix Laboratory, and the software is built around vectors and matrices. Therefore, this makes the software particularly useful for solving linear algebra problems, but also very useful for solving algebraic and differential equations and numerical integration. MATLAB has a series of graphics tools that can generate advanced GUI and data graphs in 2-D and 3-D. MATLAB also has multiple toolboxes that can be used to perform communications, signal processing, image processing, optimization, and other professional operations.

MathWorks has created an excellent online tutorial to review basic and advanced concepts, and provides instructor-led tutorials to demonstrate the various features of MATLAB. Most designers start by modeling and simulating the system using MathWorks MATLAB and Simulink.

Through the availability of a wide range of built-in functions and toolboxes, especially for signal processing and communication, developing and testing applications have become very common and widely adopted. However, in order to use these models on different platforms, developers need to use MATLAB Coder and Simulink Coder to generate C/C++ code.[4]

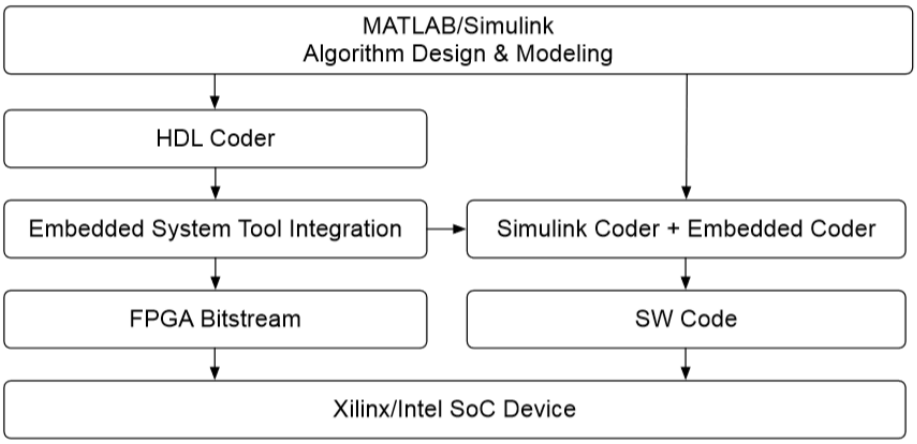

Figure1. 5:MathWorks SoC design flow.

B. Vivado HLS and SDSoC

Xilinx Vivado HLS [86] is a design environment for advanced synthesis. This tool provides a variety of functions to adjust and improve the RTL netlist output compatible and optimized with Xilinx FPGA boards. It accepts input specifications described in multiple languages (such as C, C++, System C, and OpenCL), and generates hardware modules in Verilog or VHDL. Developers can optimize regional and timing solutions by using instructions (optimization process guidelines) and RTL optimization pragmas. These optimizations include loop unrolling, loop pipeline, and operation linking. SDSoC is another tool from Xilinx.

The main difference between these two tools is that the latter has the ability to provide solutions for SoC. SDSoC is built on Vivado HLS and has the same C to RTL conversion capability. The main advantage of using SDSoC is that it will automatically generate a data mover, which is responsible for transferring data between the software on the processor and the hardware on the FPGA. An open-source tool similar to SDSoC is LegUP. [4]

C. GNU Radio

It is an open-source software development kit that provides signal processing modules to implement SDR. It runs on a desktop or laptop computer, plus simple hardware, such as USRP B200, can build a basic SDR. It is often used by academia and research communities for simulation and quick setup of SDR platforms. Similar to the System Generator tool and

Simulink, it includes different types of blocks such as decoders, demodulators, and filters. It can also connect these blocks in a reliable way and manage data transfer. In addition, it also supports the USRP system. One of the attractive features of GNU Radio is the ability to define and add new blocks. This can be done by programming in C++ or Python. [4]

D. LabVIEW

A widely used tool from National Instruments that provides a visual programming environment for test, automation, and control applications used by industry and academia. It is similar to GNU Radio and Simulink, and the design can be implemented schematically by connecting chains of various blocks, each of which performs a specific function. It also provides comp5lete support for USRP, enabling rapid prototyping of communication systems. You can use high-level languages (such as C or MATLAB) or use graphical data streams to design the different blocks of the system. [4]

E. CUDA

Developed by NVIDIA, it publishes and manages computing platforms and programming models for data parallel computing on GPUs. When the GPU is used as a coprocessor as part of the processing architecture, developers usually use CUDA and hope to take full advantage of its capabilities by accelerating applications.

In order to identify the application components that should run on GPP and the parts that should be accelerated by the GPU, we need to look at the task at hand. The programming languages that can be used in CUDA include C, C++, Python, Fortran, and MATLAB. In addition to a rich library for GPU-related acceleration functions, the toolkit also includes compilers, development tools, and CUDA runtime for developing applications and optimizing them for systems that include GPUs. [4]

6. Introduction to the USRP

The Universal Software Defined Radio Peripheral USRP N series (USRP) is the most common SDR platform known to the developer community. It provides a hardware platform for the GNU Radio project.

Two generations are available: USRP1 and USRP2. USRP1 (released in 2004) connects to a general-purpose computer via USB and adds a small FPGA. The FPGA board has two functions: routing information and limited signal processing. Due to the limitation of USB 2.0, this generation can support ~ 3MHz bandwidth. The second generation of USRP2 was released in 2008, using Gigabit Ethernet to support 25MHz bandwidth. It includes a Xilinx Spartan 3 FPGA for local processing operations. [4]

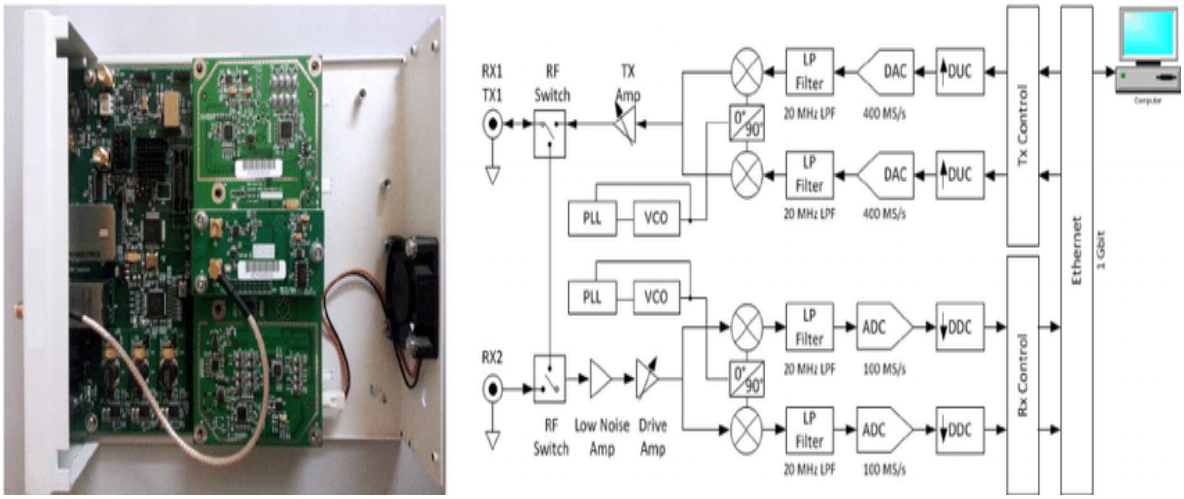

Figure1. 6:Universal Software Radio Peripheral (USRP).

USRP, generally speaking, is a board with ADC and DAC, RF front end, PC host interface and FPGA. The board consists of a motherboard and four daughter boards (two transmitters Tx and two receivers Rx), as shown in Figure 1.6.

The daughter board handles analog operations such as filtering and up/down conversion. They are modular, so they can handle applications running at frequencies up to 6GHz. The FPGA board, depending on the USRP series, handles some signal processing operations, and most of the operations are offloaded to the connected host system.

The USRP platform can be easily set up and used. However, although their performance is suitable for research experiments and rapid prototyping, these platforms do not necessarily meet the requirements of communication standards. In fact, the minimum

bandwidth of the used RF, PC host or FPGA components will affect the throughput and timing characteristics of the platform. [4]

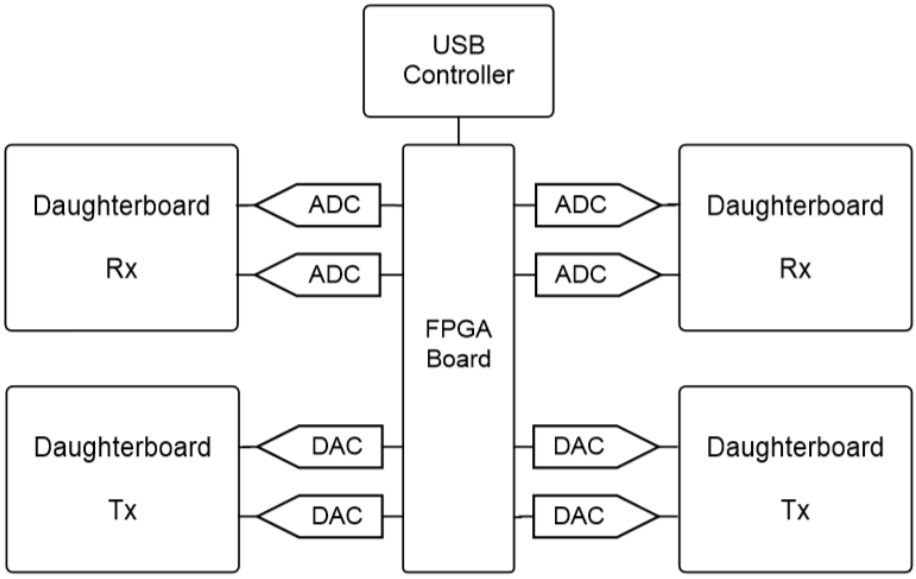

Figure1. 7:USRP board architecture. RF daughterboard selection depends on the application specifications in terms of frequency coverage.

7. NI 29xx USRPs applications

Each USRP is equipped with a VERT900 omnidirectional whip antenna, which is a dual-band antenna with rated frequencies of 824-960 MHz and 1710-1990 MHz [4]. Software-defined radio equipment USRP — USRP-2920 is a tunable radio frequency transceiver with high-speed analog-to-digital converter and digital-to-analog converter for streaming baseband I and Q signals to Host PC. [7]

We use USRP-2920 for the following applications :

- Facilitate the interaction between the computer and the user to obtain, analyze, process and present measurement data. It is either a pre-built application with predefined functions or a programming environment for building applications with custom functions. Custom applications are usually used to automate multiple functions of equipment, execute signal processing algorithms, and display custom user interfaces. [6]

- Also used for blanks; broadcast FM; public safety; land mobile, low-power unlicensed devices on the industrial, scientific, and medical (ISM) band; sensor networks; cell phones; amateur radio; or GPS. [6]

8. CONCLUSION

Software-defined radio has a wide range of advantages and functions and has attracted researchers in the past few years. Because of their modularity, versatility and Digital in nature, many new radio systems are developed in software instead of hardware. Composed of general front-end hardware modules, signal processing SDR is usually performed in a general-purpose processor with a computer. As front-end hardware and general-purpose CPUs continue to become more powerful, developers will continue to implement more advanced software radios. Therefore, in the next few years, SDR will become a more important and influential part of society. In this article, we give a comprehensive overview of the various design methods and hardware platforms used in the SDR solution. This includes GPP, GPU, DSP, FPGA and co-design. We explained the basic architecture and analyzed their advantages and disadvantages. Due to the different characteristics of the design method. [8]

CHAPITRE II

The Digital Communication Chain

1. The Digital Communication Chain

A. Introduction

In order to transmit information over long distances, the information needs to be placed in an appropriate form and "carried" by physical media: electromagnetic waves, electrical signals, light, sound waves, etc.

This format requires non-zero duration for data transmission.

In addition, the signal conveying the information may be distorted, and its harmful consequences must be minimized as much as possible. The principal diagram of the digital transmission chain is shown in Figure 2.1. We can distinguish: the source of the message, the transmission medium and the receiver are the problematic data. Source coding and decoding, channel coding and decoding, transmitters and receivers represent the freedom of the designer to implement the transmission system. We will now describe the different elements that make up the transmission chain. [6]

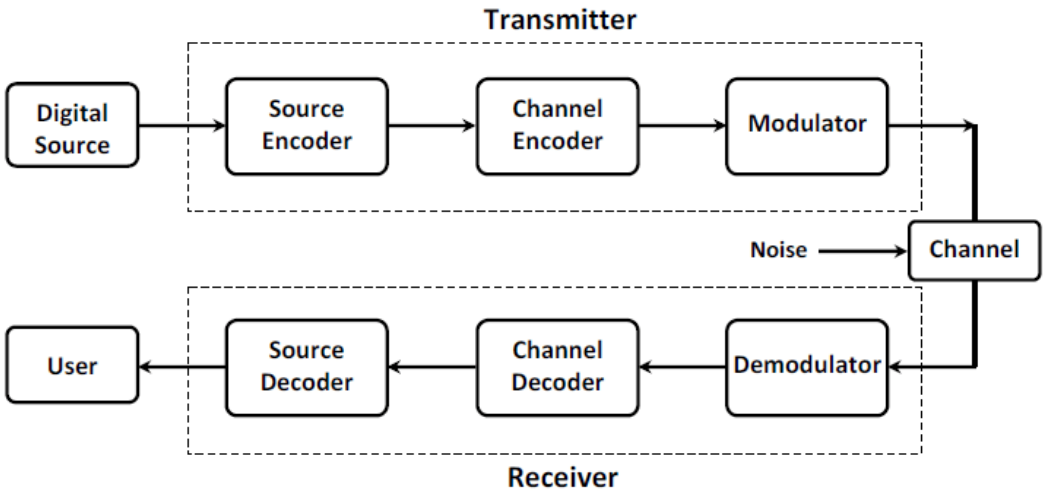

Figure2. 1:transmission Chain.

B. The message source

To achieve digital transmission, the message to be transmitted must be in digital form.
If the source delivers an analog message such as the speech (output from a microphone) or the image signal (output from a camera), it must be digitize by sampling the analog message and then quantifying the samples obtained. Each quantified sample is then encoded on M elements binary (traditionally called bits). [6]

C. Source coding

The source code encoding principle that found its foundation in the information purpose theory is to eliminate less important binary elements from the message. The latter is a succinct form, consisting of a series of mutually independent binary elements, with values of 0 and 1, and probabilities of 0 p and 1 p. To achieve digital transmission, the message to be transmitted must be in digital form. If the source transmits an analog message, such as voice (microphone output) or image signal (camera output), it must be digitized by sampling the analog message and then quantizing the obtained samples. Then encode each quantized sample into M binary elements (traditionally called bits). [6]

$$\boldsymbol{D = \frac{1}{Tb}\ (bit.S^{-1})} \qquad (2.1)$$

D. Channel coding

Channel coding, also called detector and/or error correction coding, is a specific function of digital transmission and is not equivalent in analog transmission. The purpose of this operation is to improve the transmission quality by inserting so-called redundant binary elements in the message according to the given rules. The disadvantage is that it limits the amount of information that can be used for transmission. A channel decoder that knows the coding rule used in transmission checks whether the rule is still complied with in reception. If this is not the case, it will detect the existence of transmission errors and correct these errors under certain conditions

Note: The channel coding function is not always used because it increases the complexity of the transmission equipment, thereby increasing their cost. [6]

E. The issuer

The digital message as a sequence of binary elements is abstract. Therefore, in order to transmit this message, it must be associated with a physical representation (in the form of an electrical signal). This is the main function of the transmitter and is usually referred to as modulation operation. More precisely, modulation includes the signal Si (t), i = 1... M, duration T = n Tb associated with each word of n elements output from the message binary output from M = n 2 Select among signals. Therefore, the bit rate D binary message is represented by a signal, and then we define the modulation speed R (in baud), for example the number of signals sent by the modulator per unit time:

$$R = \frac{1}{T}\ (Bauds) \qquad (2.2)$$

Then we talked about multi-ary transmission. In this case, the modulation speed R can be expressed as a function of the bit rate D, and the relationship is as follows:

$$R = \frac{D}{\log_2 M} \qquad (2.3)$$

The choice of signal type depends of course on the physical characteristics of the transmission medium through which the signal will pass; therefore, the issuer also ensures that the modulated signal is adapted to the function of the transmission medium. From the processing performed by the transmitter, we can refer to the filtering of the modulated signal to limit its frequency band, thereby allowing multiple users to share the same medium for transmission without the risk of interference

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modulated signal to limit its frequency band, thereby allowing multiple users to share the same medium for transmission without the risk of interference. [6]

F. Transmission channel

Since channels are physical devices, the signals flowing through them are always analog, even if the information is still encoded by digital messages. Transmission is often interfered by two phenomena that limit the amount of data that can be transmitted: noise, which can be electronic (generated by components), electromagnetic (due to cosmic rays) or interfere with other signals (crosstalk phenomenon); due to physical limitations of the channel or equipment Distortion caused by defects: Signal attenuation, amplitude and phase distortion, echo (multipath), limited channel bandwidth. [7]

For these reasons, as the first method, the channel is usually modeled by a low-pass filter and additional noise:

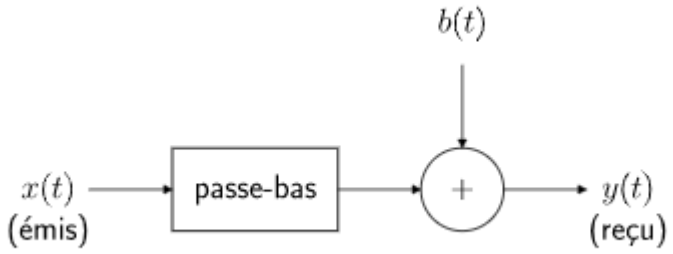

Figure2. 2: simple model of a channel.

G. The receiver

The receiver has the function of reconstructing the message sent by the source from the received signal, including amplification, frequency conversion and demodulation circuits for carrier transmission, filtering, sampling and tapping. Make a decision. Changes in frequency and demodulator can bring the modulated signal back to baseband. In order to minimize the influence of noise, which is an important source of transmission errors, the baseband signal is then filtered and then sampled at the characteristic time. Finally, the decision circuit identifies the value of the binary element transmitted from the received

sample. The choice made by the decision circuit is binary, decision 0 or decision 1, which corresponds to the so-called "detection" operation. [6]

2. Digital Modulation

A. Definition

Modulation is defined as a process in which certain characteristics of the carrier wave change according to the modulating wave. In digital communication, the modulated wave is composed of binary data or its M-ary coded version, and the carrier is a sine wave. Provide greater information capacity, higher data security, faster system availability, and high-quality communications. Therefore, compared with analog modulation technology, digital modulation technology has greater demand because they can transmit a larger amount of data.

According to needs, there are many types of digital modulation techniques and their combinations. Among them, we will discuss the prominent ones. [8]

B. Types of Digital Modulation

a. ASK – Amplitude Shift Keying

Amplitude shift keying ASK is a kind of amplitude modulation, which represents binary data in the form of signal amplitude changes.

Any modulating signal has a high-frequency carrier. When the binary signal is in ASK modulation, it provides a zero value for the low input, and provides a carrier output for the high input.

The following figure shows the ASK modulation waveform and its input. [9]

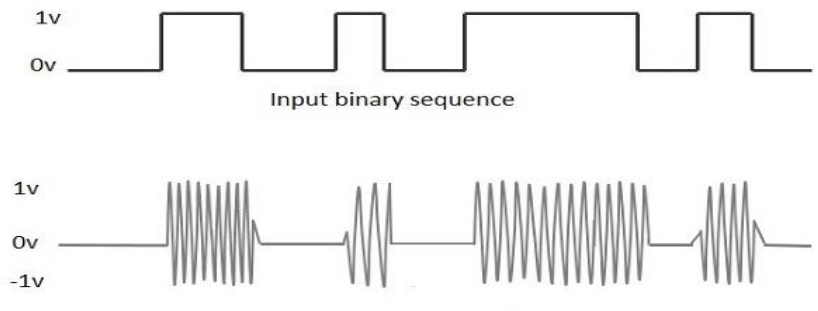

Figure2. 3: ASK modulated output wave.

In order to find the process of obtaining this ASK modulated wave, let us understand the working principle of the ASK modulator.

ASK Modulator:

The block diagram of the ASK modulator includes a carrier signal generator, a binary sequence from the message signal, and a band-limit filter. The following is the block diagram of the ASK modulator.

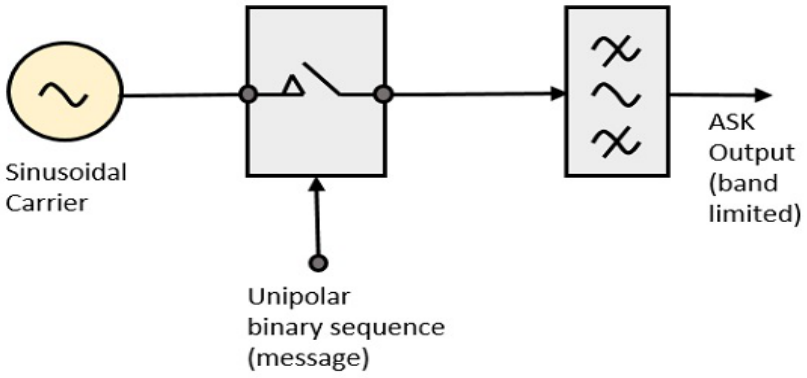

Figure2. 4: ASK generation method.

The carrier generator sends a continuous high frequency carrier. The binary sequence from the message signal makes the unipolar input high or low. The high signal turns off the switch, allowing the carrier. Therefore, the output will be the carrier signal at high input. When the input is low, the switch opens and no voltage is allowed. Therefore, the output will be very low. The band limit filter shapes the pulse according to the amplitude and phase characteristics of the band limit filter or pulse shaping filter. [9]

ASK Demodulator

There are two types of ASK Demodulation techniques. They are:

- Asynchronous ASK Demodulation/detection.
- Synchronous ASK Demodulation/detection.

When the clock frequency of the transmitter matches the clock frequency of the receiver, it is called a synchronization method because the frequency will be synchronized. Otherwise, it is called asynchronous.[9]

1. Asynchronous ASK Demodulator:

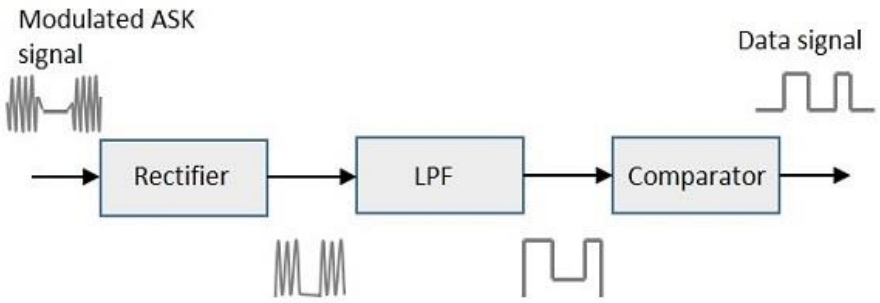

Figure2. 5: asynchronous ASK detector.

The asynchronous ASK detector consists of a half-wave rectifier, a low-pass filter and a comparator. The following is the same block diagram.

The modulated ASK signal is provided to the half-wave rectifier, which provides a positive half output. The low-pass filter suppresses higher frequencies and provides an envelope detection output from which the comparator provides a digital output. [9]

2. Synchronous ASK Demodulator:

The synchronous ASK detector consists of a square law detector, a low-pass filter, a comparator and a voltage limiter. The following is the same block diagram.

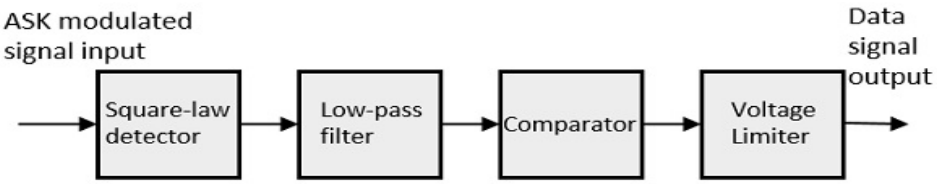

Figure2. 6:synchronous ASK detector.

The ASK modulated input signal is provided to the square law detector. The output voltage of the square law detector is proportional to the square of the amplitude modulated input voltage. The low-pass filter minimizes higher frequencies. The comparator and voltage limiter help to obtain a clean digital output. [9]

b. Frequency Shift Keying

FSK is a digital modulation technique in which the frequency of the carrier signal changes with the change of the digital signal. FSK is a frequency modulation scheme. The output of FSK modulation wave is high for binary high input frequency and low for binary low input frequency. The binary ones and zeros are called marker frequency and spatial frequency.

The figure below is a schematic diagram of FSK modulation waveform and its input. To find the process of obtaining this FSK modulated wave, please let us understand the working principle of the FSK modulator. [9]

FSK Modulator:

The FSK modulator block diagram includes two oscillators with a clock and input binary sequence. Below is its block diagram.

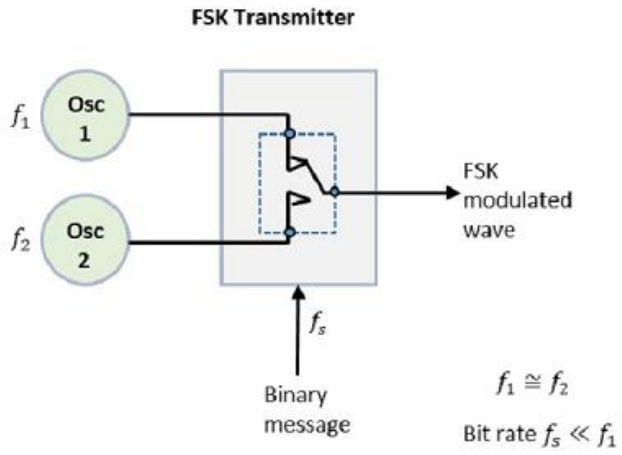

Figure2. 7:FSK Transmiter.

Two oscillators that generate higher and lower frequency signals are connected to the switch along with the internal clock. To avoid sudden phase discontinuities of the output waveform during message transmission, the clock is internally applied to the two oscillators. The binary input sequence is applied to the transmitter to select the frequency based on the binary input. [9]

FSK Demodulator:

There are different ways to demodulate FSK waves. The main methods of FSK detection are asynchronous detectors and synchronous detectors. Synchronous detectors are coherent detectors, while asynchronous detectors are non-coherent detectors. [9]

1) Asynchronous FSK Detector:

The block diagram of the asynchronous FSK detector consists of two band-pass filters, two envelope detectors and a decision circuit. The following is a schematic diagram.

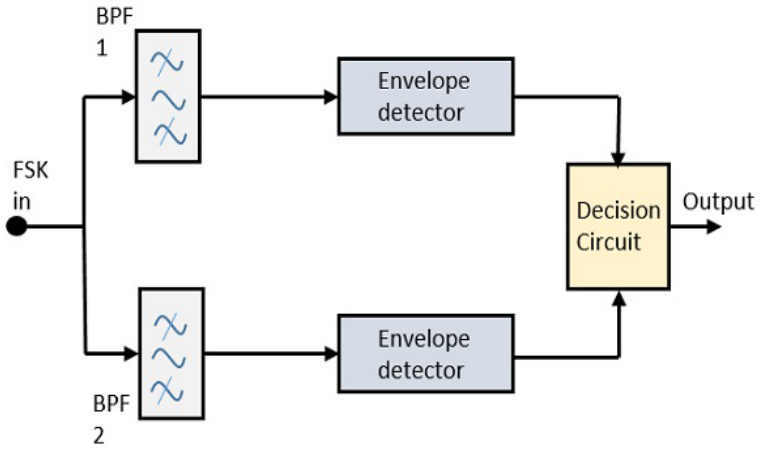

Figure2. 8:Asynchronous FSK Detector.

The FSK signal passes through two band-pass filters BPFs BPF, tuned to the spatial and marker frequencies. The output of these two BPFs looks like an ASK signal, which is provided to the envelope detector. The signal in each envelope detector is asynchronously modulated. The decision circuit selects the more likely output and selects it from any envelope detector. It also reshapes the waveform into a rectangle. [9]

2. Synchronous FSK Detector:

The block diagram of the synchronous FSK detector consists of two mixers with local oscillator circuits, two bandpass filters, and a decision circuit. The following is a schematic diagram.

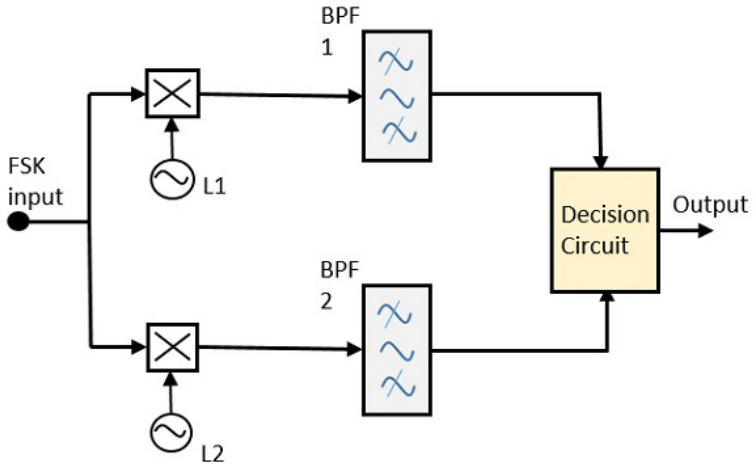

Figure2. 9:synchronous FSK Detector.

The FSK signal input is provided to two mixers with local oscillator circuits. These two are connected to two bandpass filters. These combinations act as demodulators, and the decision circuit selects the more likely output and chooses from any one of the detectors. These two signals have the smallest frequency separation.

For two demodulators, the bandwidth of each demodulator depends on their bit rate. This synchronous demodulator is slightly more complicated than the asynchronous demodulator. [9]

c. Phase Shift Keying PSK

PSK is a digital modulation technique that changes the phase of the carrier signal by changing the sine and cosine inputs at a specific time. PSK technology is widely used in wireless local area networks, biometrics, contactless operations, and RFID and Bluetooth communications. There are two types of PSK, depending on the phase of the signal offset. They are:

1. Binary Phase Shift Keying BPSK:

This is also called 2-phase PSK or phase reversal keying. In this technique, the sine wave carrier requires two phase reversals, such as 0° and 180°. BPSK is basically a double-

sideband suppressed carrier DSBSC modulation scheme, because the message is digital information. [9]

- **BPSK Modulator:** he block diagram of binary phase shift keying consists of a balanced modulator that takes a carrier sine wave as one input and a binary sequence as the other input. The following is a schematic diagram.

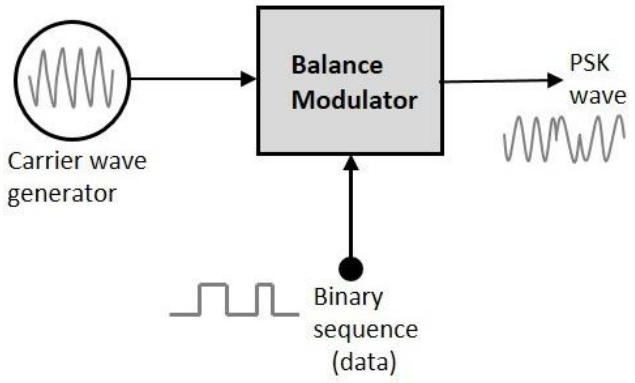

Figure2. 10:BPSK Modulator.

The modulation of BPSK is done using a balanced modulator, which multiplies the two signals applied to the input. For a zero binary input, the phase will be 0°, and for a high input, the phase will be reversed to 180°. The following is an illustration of the BPSK modulated output wave and its given input. [9]

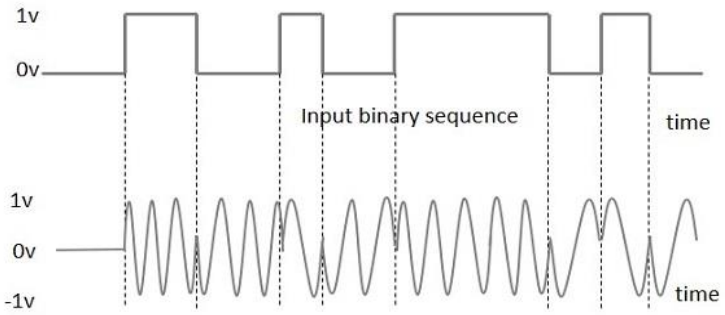

Figure2. 11:BPSK modulated output wave.

The output sine wave of the modulator will be the direct input carrier or the reverse 180° phase shift 180° phase shift input carrier, which is a function of the data signal. [9]

- **BPSK Demodulator:** The block diagram of the BPSK demodulator consists of a mixer with a local oscillator circuit, a band-pass filter, and a two-input detector circuit. The schematic diagram is as follows.

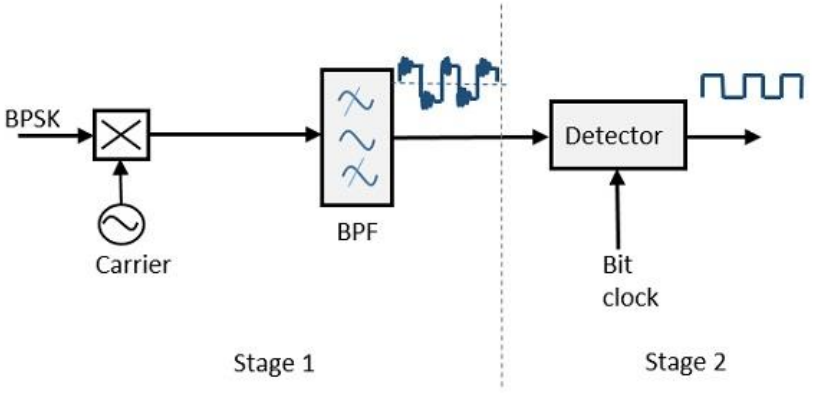

Figure2. 12:BPSK demodulator.

By recovering the band-limited message signal, with the help of the mixer circuit and the band-pass filter, the first stage of demodulation is completed. Obtain a band-limited baseband signal, which is used to regenerate the binary message bit stream. In the next stage of demodulation, the bit clock rate is determined at the detector circuit to generate the original binary message signal. If the bit rate is a divisor of the carrier frequency, then the bit clock regeneration is simplified. In order to make the circuit easy to understand, you can also insert a decision circuit in the second stage of the test. [9]

1. Quadrature Phase Shift Keying QPSK:

This is the phase shift keying technology, in which the sine wave carrier undergoes four phase inversions of 0°, 90°, 180° and 270°. If this technique is further expanded, PSK can also be completed with eight or sixteen values, depending on the requirements
Quadrature Phase Shift Keying QPSK is a variant of BPSK, and it is also a double-sideband suppression carrier DSBSCDSBSC modulation scheme, which sends two-digit information

at a time, called bigits. Instead of converting digital bits into a series of digital streams, it converts them into bit pairs. This reduces the data bit rate to half, thus providing space for other users. [9]

- **QPSK Modulator:**

The QPSK modulator uses a bit splitter, two multipliers with local oscillators, a 2-bit serial-to-parallel converter and an adder circuit. The following is the same block diagram [13].

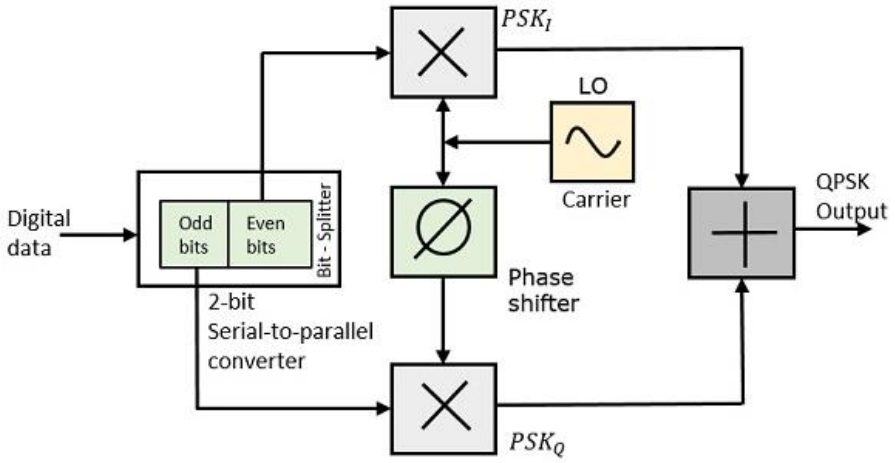

Figure2. 13:QPSK Modulator.

At the input of the modulator, the even-numbered bits (i.e., the second, fourth, sixth, etc.) and odd-numbered bits (i.e., the first, third, fifth, etc.) of the message signal are divided by the bit separator and multiply the same carrier to generate odd BPSK (called PSKI) and even BPSK (called PSKQ). In any case, the PSKQ signal is phase shifted by 90° before modulation.

The QPSK waveform of the two-digit input is shown below, showing the modulation results of different binary input instances. [9]

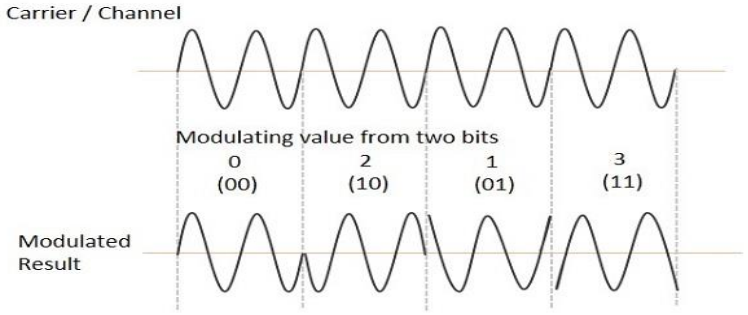

Figure2. 14:QPSK modulated output wave.

❖ ***QPSK Demodulator:***

The QPSK demodulator uses two product demodulator circuits with local oscillators, two bandpass filters, two integrator circuits, and a 2-bit parallel-to-serial converter. Below is the same chart. [9]

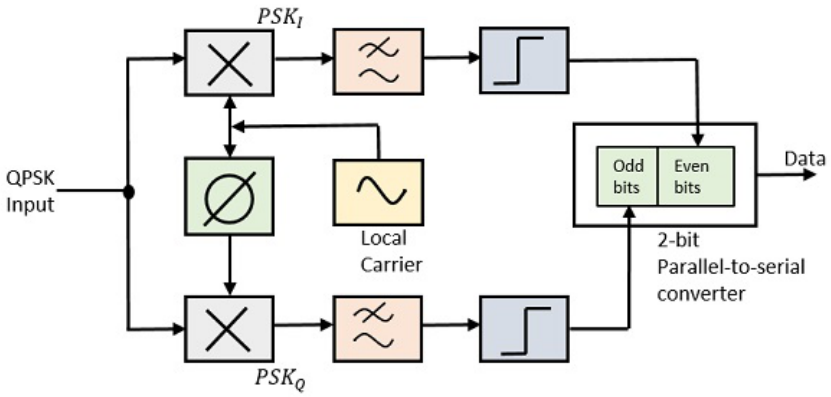

Figure2. 15:QPSK demodulator.

Two product detectors at the input of the demodulator demodulate two BPSK signals simultaneously. The pair is restored from the original data here. After these signals are processed, they are passed to the parallel-to-serial converter. [9]

2. Differential Phase Shift Keying DPSK:

The phase of the DPSK modulated signal is shifted relative to the previous signal element. The reference signal is not considered here. The signal phase follows the high or low state of the previous element. This DPSK technique does not require a reference oscillator. The figure below shows the model waveform of DPSK. [9]

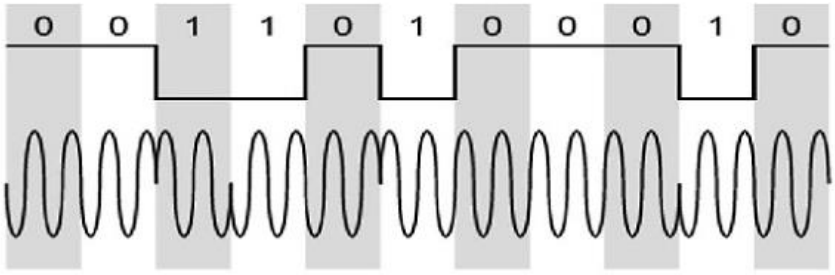

Figure2. 16: DPSK modulated output wave.

As can be seen from the above figure, if the data bit is Low, that is, 0, the phase of the signal is not reversed, but continues as it is. If the data is high, that is 1, the phase of the signal is reversed, and like NRZI, it is reversed on 1.

If we observe the above waveform, we can say that the High state represents M in the modulated signal, and the Low state represents W in the modulated signal. [9]

- **DPSK Modulator:**

DPSK is a technology of BPSK in which there is no reference phase signal. Here, the transmitted signal itself can be used as a reference signal. The figure below is a schematic diagram of the DPSK modulator. [9]

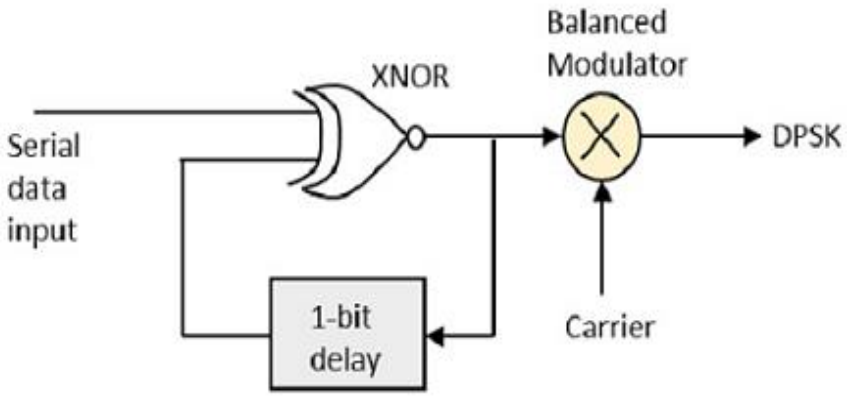

Figure2. 17:DPSK modulator.

DPSK encodes two different signals, that is, the carrier and the modulated signal each have a phase shift of 180°. The serial data input is provided to the XNOR gate, and the output is fed back to the other input again with a 1-bit delay. The output of the XNOR gate is supplied to the balanced modulator together with the carrier signal to generate the DPSK modulated signal. [9]

- **DPSK Demodulator:**

In the DPSK demodulator, the phase of the inverted bit is compared with the phase of the previous bit. The following is the block diagram of the DPSK demodulator. [13]

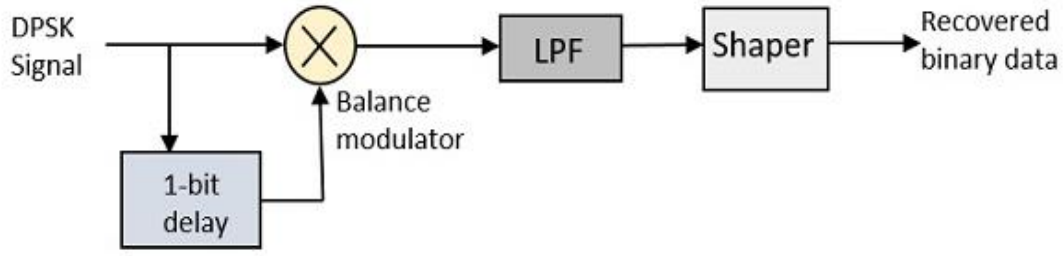

Figure2. 18:DPSK demodulator.

As can be seen from the figure above, the balanced modulator is given a DPSK signal and a 1-bit delay input. With the help of LPF, the signal is limited to a lower frequency. It is

then passed to a shaper circuit, which is a comparator or Schmitt trigger circuit, to restore the original binary data as output.

The word binary stands for two bits. M represents a number, which corresponds to the number of possible conditions, levels, or combinations of a given number of binary variables.

This is a digital modulation technique used for data transmission in which two or more bits are transmitted at a time instead of one bit. Since a single signal is used for multi-bit transmission, the channel bandwidth is reduced. [9]

d. Quadrature Amplitude Modulation QAM

In view of the fact that QAM provides fast information and effective spectral density, Quadrature Amplitude Modulation (QAM) is commonly used in systems that transmit discrete multi-location signals over wired and radio channels. However, the basic QAM signal demodulation gadget has several disadvantages. The first one is to use simple symbol processing, which needs to pay for adequate differentiation of orthogonal channels and some other errors. [10]

The other is the complexity of the digitally executed signal processing, including a large number of mathematical tasks to manage each sample of the received signal, which indicates the need for expensive high-speed equipment. What is important is that a general algorithm has been created for demodulation of QAM signals in changing information transmission systems. Nevertheless, for this situation, their execution may require critical computing assets. [11]

- **QAM modulator basics:** The QAM modulator essentially follows the idea that can be seen from the basic QAM theory, where there are two carrier signals, and the phase shift between them is 90°. They are then amplitude modulated with two data streams called I or in-phase and Q or quadrature data streams. These are generated in the baseband processing area. [12]

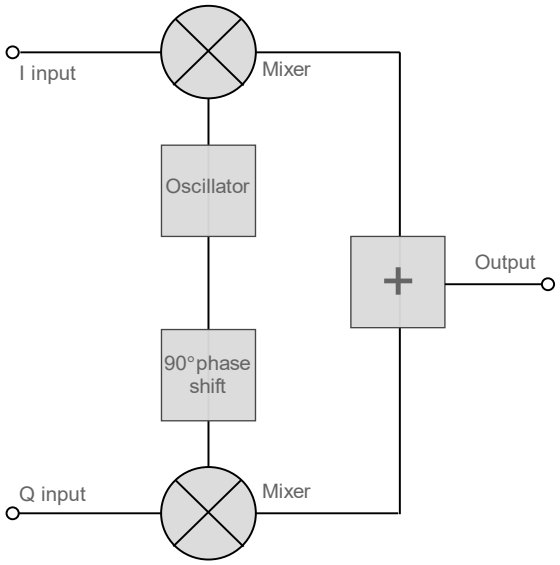

Figure2. 19:QAM modulator.

- **<u>QAM demodulator basics:</u>** The QAM demodulator is the exact opposite of the QAM modulator. The signals enter the system, they are separated and applied to the mixer on each side. Half use the in-phase local oscillator, and the other half use the quadrature oscillator signal. [12]

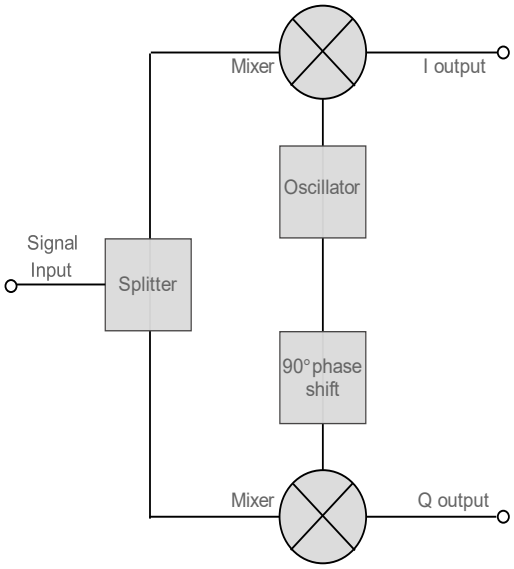

Figure2. 20:QAM demodulator.

The basic modulator assumes that the two orthogonal signals remain completely orthogonal. Another requirement is to derive the local oscillator signal for demodulation,

which is exactly at the frequency required by the signal. Any frequency offset will be the phase change of the local oscillator signal relative to the two double sidebands of the entire signal to suppress the carrier component. The system includes circuits for carrier recovery, usually phase-locked loops-some even have inner and outer loops. It is important to recover the phase of the carrier, otherwise the bit error rate of the data will be affected. The circuit shown above shows common IQ QAM modulator and demodulator circuits used in a large number of different fields. These circuits are not only made of discrete components, but are more commonly used in integrated circuits that can provide a large number of functions. [12]

e. M-ary Equation

If a digital signal is given under the four conditions of voltage level, frequency, phase and amplitude, then **M = 4.**

The number of digits required to produce a given quantity condition is expressed mathematically as

$$N = MN = log2\ M \qquad (2.4)$$

Were

N is the number of bits necessary

M is the number of conditions, levels, or combinations possible with **N** bits.

The above equation can be re-arranged as

$$2^N = M \qquad (2.5)$$

For example, with two bits, $\mathbf{2^2 = 4}$ conditions are possible. [9]

1. Types of M-ary Techniques:

Generally speaking, multi-level M-ary modulation technology is used for digital communication because digital inputs with more than two modulation levels are allowed on the input of the transmitter. Therefore, these techniques are bandwidth efficient.

There are many M-ary modulation techniques. Some of these techniques modulate a parameter of the carrier signal, such as amplitude, phase, and frequency. [9]

1.1. M-ary ASK:

This is called M-ary amplitude shift keying M-ASKM-ASK or M-ary pulse amplitude modulation PAM.

The amplitude of the carrier signal has M different levels.

1.1.1. Representation of M-ary ASK:

$Sm(t) = Amcos(2\pi fct)$ (2.6)

Amϵ(2m−1−M) Δ, m=1, 2....M and 0≤t≤Ts

Some prominent features of M-ary ASK are −

- This method is also used in PAM.
- Its implementation is simple.
- M-ary ASK is susceptible to noise and distortion.

1.2. M-ary ASK:

This is called M-ary Frequency Shift Keying M-aryFSK. The frequency of the carrier signal has M different levels. [9]

1.2.1. Representation of M-ary FSK:

$$Si(t) = \sqrt{\frac{2Es}{Ts}} \cos\left(\frac{\pi}{Ts}(nc + i)t\right) \qquad (2.7)$$

0≤t≤Ts and i=1,2, 3....M 0≤t≤Ts and i=1,2, 3....M

Where fc=nc2Tsfc=nc2Ts for some fixed integer n.

Some prominent features of M-ary FSK are:

- Not susceptible to noise as much as ASK.
- The transmitted M number of signals are equal in energy and duration.
- The signals are separated by 12Ts12Ts Hz making the signals orthogonal to each other.
- Since M signals are orthogonal, there is no crowding in the signal space.
- The bandwidth efficiency of M-ary FSK decreases and the power efficiency increases with the increase in M. [9]

1.3. M-ary PSK:

This is called M-ary phase shift keying M-aryPSK.

The phase of the carrier signal has M different levels. [9]

1.3.1. Representation of M-ary PSK:

$$Si(t) = \sqrt{\frac{2E}{T}}\cos\left(w0t + \varphi it\right) \qquad (2.8) \qquad 0\leq t\leq T$$

and i=1,2...M

$$\varphi i(t) = \frac{2\pi i}{M} \qquad (2.9) \qquad \text{Where}$$

i=1,2,3.....M

Some outstanding features of M-ary PSK are-

- The envelope is constant, with more phase possibilities.
- This method was used in the early days of space communication.
- Better performance than ASK and FSK.
- The minimum phase estimation error of the receiver.

- The bandwidth efficiency of M-ary PSK decreases, and the power efficiency increases as M increases.

So far, we have discussed different modulation techniques. The output of all these technologies is a binary sequence, represented by 1 and 0. There are many types and forms of this binary or digital information, which will be discussed further. [9]

3. Wireless channels

A. The types of wireless channels

can be summarized as follows:

a. Direct view transmission waves

Laser or IR rays:

- Communication between 2 nearby buildings
- Very direct digital transmission [13].

Radio waves :

- Long-distance communication between direct-viewing parabolic antennas is more than 10 kilometers (100 meters high tower is 100 kilometers range)
- The main artery of the telephone network and TV
- Poor link quality due to interference, multipath, and weather conditions
- The bandwidth is divided into several frequency bands for use in public networks (4-6Ghz), military, government organizations [13]

b. Communication satellites

Satellite communication, in telecommunications, uses artificial satellites to provide communication links between points on the earth. Satellite communications play a vital role in the global telecommunications system. Approximately 2,000 artificial satellites orbiting the earth relay analog and digital signals and transmit voice, video and data to one or more locations around the world.

Satellite communication has two main components: the ground part, including fixed or mobile transmission, reception and auxiliary equipment, and the space part, mainly the satellite itself. A typical satellite link involves signal transmission or uplink from the earth station to the satellite. The satellite then receives and amplifies the signal and retransmits it back to the earth, where it is received and re-amplified at the earth station and terminal. Satellite receivers on the ground include direct-to-home (DTH) satellite devices, mobile receivers on airplanes, satellite phones, and handheld devices. [14]

B. Propagation in the wireless channel

Satellite communication, in telecommunications, uses artificial satellites to provide communication links between points on the earth. Satellite communications play a vital role in the global telecommunications system. Approximately 2,000 artificial satellites orbiting the earth relay analog and digital signals and transmit voice, video and data to one or more locations around the world.

Satellite communication has two main components: the ground part, including fixed or mobile transmission, reception and auxiliary equipment, and the space part, mainly the satellite itself. A typical satellite link involves signal transmission or uplink from the earth station to the satellite. The satellite then receives and amplifies the signal and retransmits it back to the earth, where it is received and re-amplified at the earth station and terminal. Satellite receivers on the ground include direct-to-home (DTH) satellite devices, mobile receivers on airplanes, satellite phones, and handheld devices. [14]

The propagation of radio waves from the transmitter to the receiver is affected by three physical phenomena: reflection, diffraction, and dispersion, as shown in the figure below. [13]

a. Reflection:

This is the reflection of EM (electromagnetic) waves on objects (earth, buildings...) whose size is larger than the wavelength. The signal strength is returned to the sender and does not reach the receiver. [13]

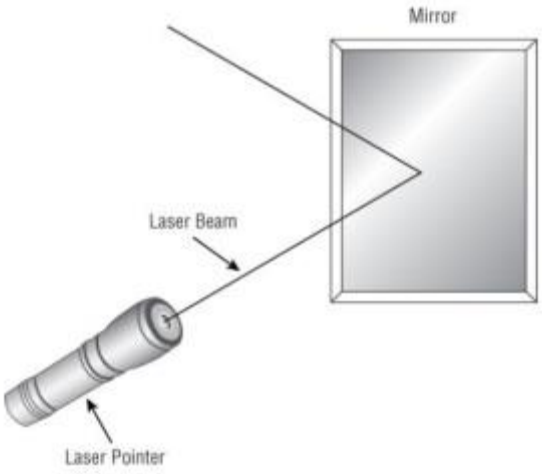

Figure2. 21:Reflection.

b. Diffraction:

It appears when EM waves encounter irregularly shaped obstacles or OEMs pass through small openings. This can cause the OEM to bend around obstacles or scatter through small openings. OEM and acquisition are very useful. When the transmitter and receiver are out of sight, it allows a path to be generated between the transmitter and receiver. [13]

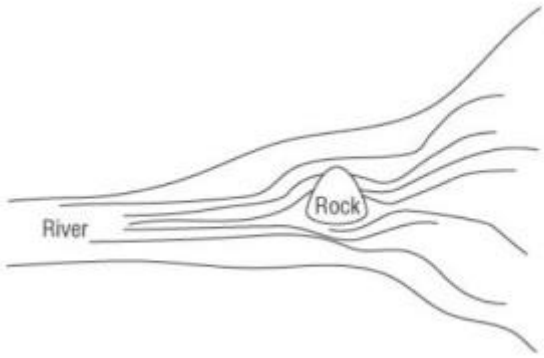

Figure2. 22:Diffraction.

c. Scattering:

This is a phenomenon of direct path deviation. The size of small obstacles is small relative to the wavelength (leaf, signal panel...). These phenomena will cause signal fading and gray areas (shadow). [13]

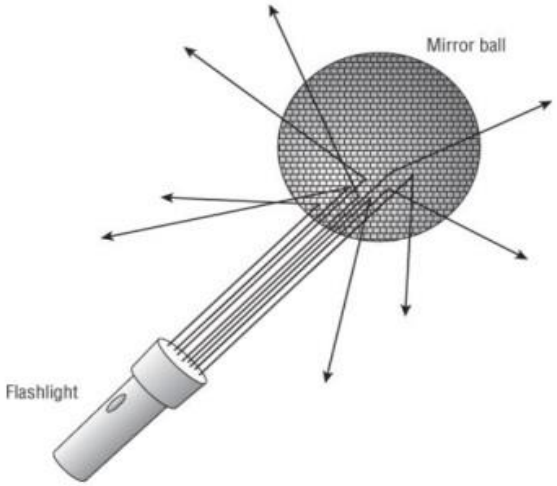

Figure2. 23: Scattering

C. Channel to fainting:

Fading phenomenon is a phenomenon in which signal amplitude changes with time and frequency, and can be divided into two types. Large-scale syncope and small-scale syncope [13]:

a. Large-scale fainting

Large-scale fading is characterized by signal attenuation as a function of distance and shadows (shaded areas caused by large obstacles such as buildings, tree……). [13]

b. Small-scale fainting

Small-scale fading is a rapid change in signal level caused by constructive or distracted multipath interference when the mobile station moves over a small distance. This leads to selective or non-selective attenuation of frequency. The interviewee's channel changes over time. Due to the movement of the mobile phone (Doppler phenomenon), small-scale syncope can be divided into fast or slow syncope.

The following figure classifies the types of fading channels.

The relationship between large-scale and small-scale fading is shown in the figure below. Large-scale fading is represented by the average attenuation that decreases with distance

and the shading around the average. Due to shading, the power signal received at the same distance from the transmitter may be different. Small-scale fading causes a brief change in the signal strength that has been affected by the shadow. [13]

D. Specific models of wireless channels for large fading scale and small scale

The power received in a line-of-sight transmission (Line-Of-Sight LOS), is (Friis equation)

a. Types of Mitigation:

The types of attenuation suffered by a radio signal during its transmission on a channel without thread are:

1) <u>Path Loss</u>:

Path loss (PL) refers to the loss or attenuation encountered by propagating an electromagnetic signal (or wave) along its path from transmitter to receiver. Due to path loss, the received signal power level is several orders of magnitude lower than the transmitted power level. The received power level depends on factors such as the transmit power, antenna gain, operating frequency, and the distance between the transmitter and receiver. Like any other gain or attenuation, path loss is also expressed in decibels (dB). We can relate the received power level to the path loss, but before that, let us know the expression of the path loss. [15]

2) <u>Shadowing: (mask effect):</u>

Shadow is an informal way to let people understand what it feels like to perform a particular job in the workplace. A person follows or stalks the worker who has already assumed that role. Work internships can be provided for new employees or junior employees, but they may also be used by horizontal employees from other departments of the organization who need to learn quickly in new roles. The shadow's time is limited, or only lasts when necessary-that is, until the new person who joins the role feels comfortable enough to take responsibility on their own. [16]

3) Fast Fading:

Fast fading is used to describe the channel whose channel coherence time <transmission symbol time. Fast fading describes a condition in which the duration of channel operation in a correlated manner is relatively short compared to the duration of the symbol. Therefore, it can be expected that in the process of symbol propagation, the fading characteristics of the channel will change many times, resulting in distortion of the baseband pulse waveform. Similar to the distortion described as ISI, distortion occurs because the components of the received signal are not all highly correlated throughout the time period. Therefore, fast fading can cause baseband pulse distortion, resulting in SNR loss, which usually results in an irreducible error rate. In addition to being difficult to fully define matched filters, such distorted pulses can also cause synchronization problems (phase-locked loop receiver failure). [17]

E. Types of channels:

a. only one direct path:

Gaussian channel. [13]

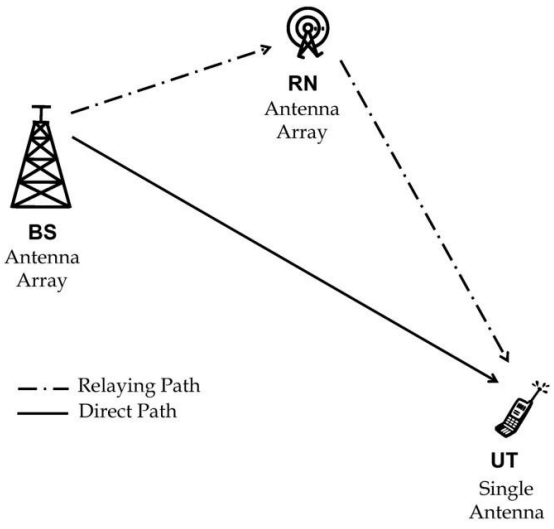

Figure2. 24:Gaussian channel.

b. existence of a line of sight (LOS propagation: Line of Sight):

Rice canal. [13]

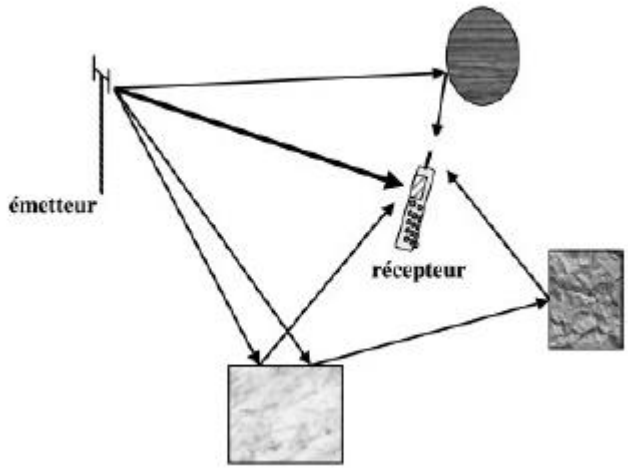

Figure2. 25:LOS propagation

c. no line of sight (NLOS propagation):

Rayleigh channel. [13]

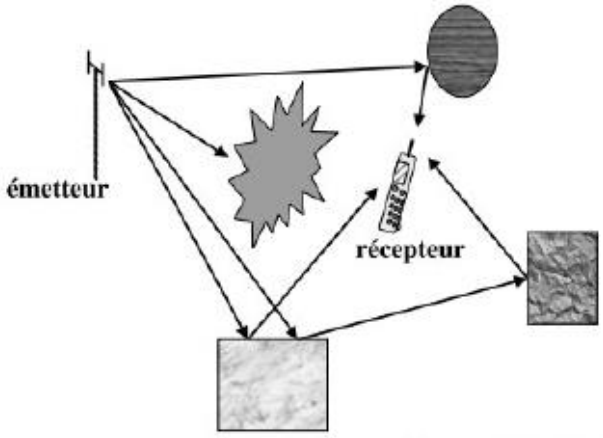

Figure2. 26:NLOS propagation.

4. OFDM:

A. Definition

Orthogonal Frequency Division Multiplexing (OFDM) is a transmission technology that consists of many orthogonal carriers that are transmitted simultaneously. The main idea behind OFDM is that a signal with a long symbol duration is less sensitive to multipath fading than a signal with a short symbol duration. Therefore, performance gains can be achieved by sending multiple parallel symbols with a longer symbol time instead of sending them in a serial manner with a shorter symbol time. The basic technology of OFDM has been known for about 40 years, but OFDM has not been widely used until recently. Products that use OFDM are WiMAX, WLAN (Wireless Local Area Network) 802.11, x-DSL (x Digital Subscriber Line) and DVT (Digital Video Broadcasting). [18]

a. Orthogonality

Conceptually, OFDM is a specialized FDM, and the additional constraint is that all carrier signals are orthogonal to each other. Orthogonality simplifies the recovery of N data streams, and orthogonal sub-carriers means there is no inter-carrier interference (ICI). Orthogonal

A function set is a set whose characteristic is that a specific operation performed between any two different members of the set produces zero. If the vectors are at right angles to each other, they are orthogonal. The dot product of any two different vectors is zero. The time domain and frequency domain orthogonality of OFDM is shown in Figure 2.27. [19]

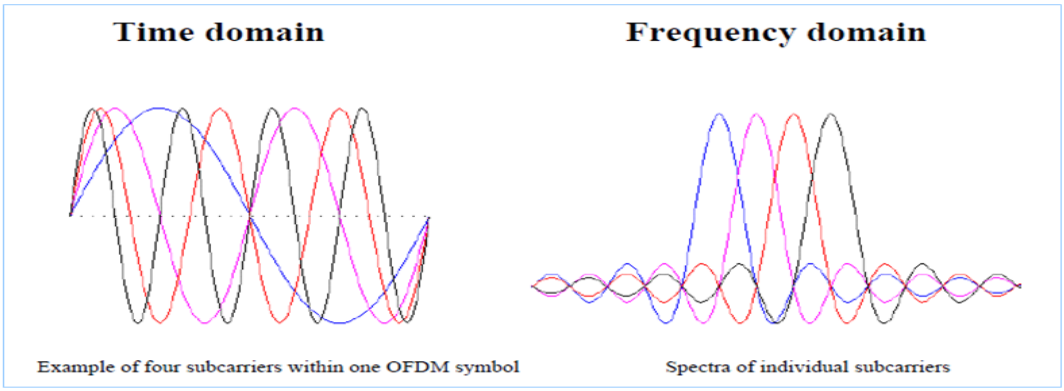

Figure2. 27:OFDM Orthogonality.

1) Time domain orthogonality:

Each subcarrier has an integer number of cycles T_{OFDM}.Satisfy The precise mathematical definition of the orthogonality of complex exponential (and sine) functions in the interval $[0, T_{OFDM}]$.

2) Frequency Domain Orthogonality:

If the FDM system has been able to use a set of mutually orthogonal sub-carriers, and as long as the orthogonality is maintained, a single sub-carrier signal can still be recovered, because if the two deterministic dot product signals are equal to 0, these signals are said to be orthogonal to each other. Orthogonality can It can also be viewed from the perspective of a random process. If two random processes are not related, they are orthogonal. Given the randomness of signals in communication systems, this probabilistic view of orthogonality provides an intuitive understanding of the meaning of orthogonality in OFDM. [19]

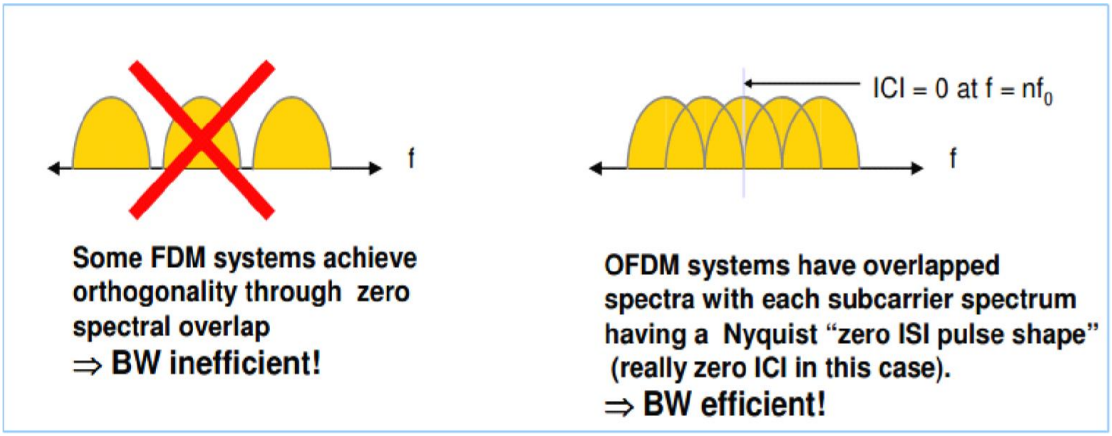

Figure2. 28:Frequency Domain Orthogonality.

B. Basic principles of OFDM:

OFDM consists of many orthogonal carriers; each carrier is called a subcarrier or tone, depending on the literature. Usually some kind of QAM (Quadrature Amplitude Modulation) is used to modulate the symbols transmitted on the subcarriers. When a symbol is transmitted on a subcarrier, its transmission time is extended by N times. However, the symbol rate is not reduced because there are N subcarriers transmitting N symbols during the time interval NT, where T is the original symbol rate. All symbols transmitted during the time interval NT form OFDM symbols.

The advantage of the OFDM system is that it can completely eliminate ISI (Inter-Symbol Interference) between OFDM symbols. ISI is usually removed by adding a cyclic prefix to the OFDM symbol before transmission. One disadvantage of the OFDM system is that due to the Doppler shift and the different frequencies in the local oscillators of the transmitter and receiver, the subcarriers are usually not orthogonal when received at the receiver. Therefore, the frequency offset must be estimated. [18]

Since ISI can be removed; each sub-carrier will only experience a flat fading channel. This statement also applies to FDM systems (frequency division multiplexing), but in FDM, there is a guard band between each carrier. There is no guard band in OFDM, and even different sub-carriers share some spectrum, as shown in Figure 2.29. [18]

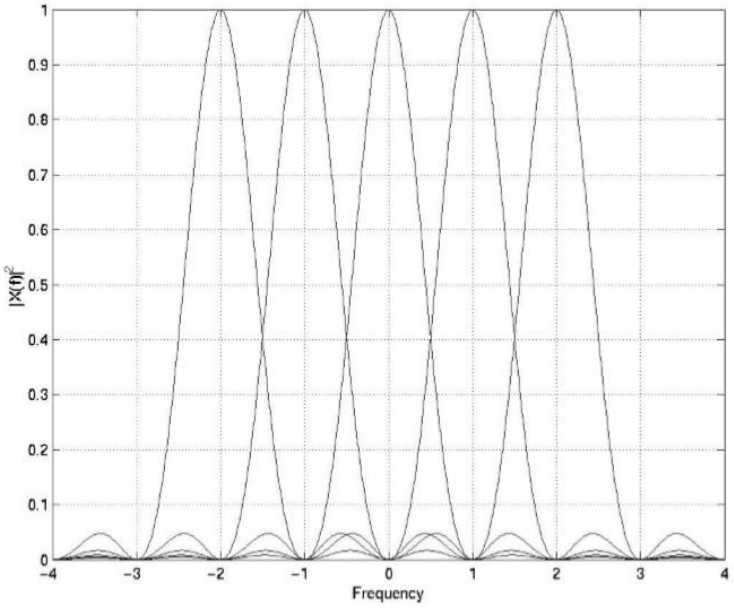

Figure2. 29:OFDM spectra.

There are five subcarriers in Figure 2.29, and each subcarrier overlaps all other subcarriers in some parts. However, the receiver can still extract the symbols sent on each sub-carrier because the sub-carriers are orthogonal, that is, when the energy of each sub-carrier is maximum, no other sub-carriers contribute any energy.

The baseband OFDM system model can be expressed in the following way, in which the form of each subcarrier is:

$e^{j2\pi f_k n}$ (2.10)

Where n is the discrete time variable and k f is the carrier frequency of the subcarrier k. The subcarrier frequency k f is defined as:

$f_{k=\frac{k}{NT}}$ (2.11)

where N is the number of subcarriers and T is the original sample time of the transmitted symbol. The baseband model of an OFDM system in discrete time is:

$x(n) = \sum_{K=0}^{N-1} c(k) e^{j2\pi f_k n}$ (2.12) 0≤n≤N-1

However, there is a problem with using the guard interval to remove ISI, which is related to the properties of DFT. DFT is cyclic, so if the received OFDM symbol is not cyclic, it will

cause ICI (Inter Carrier Interference) between sub-carriers. The solution is to add cyclic extension to the OFDM symbol before transmission. The cyclic extension added before transmission is just the end of the OFDM symbol copied and transmitted before the OFDM symbol, as shown in Figure 2.29. The cyclic extension is called CP (Cyclic Prefix). [18]

C. working principle:

However, there is a problem with using the guard interval to remove ISI, which is related to the properties of DFT. DFT is cyclic, so if the received OFDM symbol is not cyclic, it will cause ICI (Inter Carrier Interference) between sub-carriers. The solution is to add cyclic extension to the OFDM symbol before transmission. The cyclic extension added before transmission is just the end of the OFDM symbol copied and transmitted before the OFDM symbol, as shown in Figure 2.30. The cyclic extension is called CP (Cyclic Prefix). [18]

Figure2. 30:Remove ISI through guard interval.

However, there is a problem with using the guard interval to remove ISI, which is related to the properties of DFT. DFT is cyclic, so if the received OFDM symbol is not cyclic, it will cause ICI (Inter Carrier Interference) between sub-carriers. The solution is to add cyclic extension to the OFDM symbol before transmission. The cyclic extension added before transmission is just the end of the OFDM symbol copied and transmitted before the OFDM symbol, as shown in Figure 2.31. The cyclic extension is called CP (Cyclic Prefix). [18]

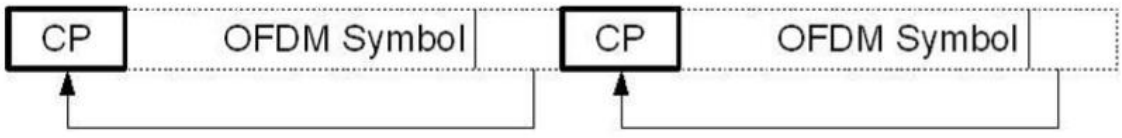

Figure2. 31:Cyclic Prefix

The length of the CP is set to at least the maximum length of the multipath delay of the radio channel, that is, at least the same as the number of taps of the channel. The corresponding baseband model of the OFDM system with cyclic prefix is

$x(n) = \sum_{k=0}^{N-1} c(k) e^{j2\pi f_k n}$ (2.13) -CP≤ n ≤ N-1

Where CP represents the length of the cyclic prefix. The disadvantage of the cyclic prefix is that it does not carry any new data, which reduces the transmission energy of each information bit, thereby reducing the SNR. [18]

D. OFDM in systems

We begin this section by describing some aspects that must be considered when implementing an OFDM system, and continue to introduce the more important aspects for the master's thesis. In most mobile communication systems, not only OFDM systems, but also some kind of channel coding is used to reduce the bit error rate by creating redundancy. This is also true for most OFDM systems, because the overhead of channel coding is usually much less than the overhead of having to retransmit the error information.

Usually two-way communication is required, that is, communication between the BS (base station) and the terminal, and vice versa. The two main methods in OFDM are FDD (Frequency Division Duplex) and TDD (Time Division Duplex). In the FDD system, downlink (from base station to terminal) and uplink (from terminal to base station) communications are separated in two different frequency bands. In the TDD system, the downlink and uplink communications are on the same frequency band, but are separated in time, for example, they are first transmitted in the downlink and then in the uplink. [18]

As mentioned earlier, some kind of channel coding is usually used to reduce the bit error rate. However, the OFDM system still needs a frequency offset estimator and a channel estimator to achieve acceptable performance. A frequency offset estimator is needed to offset the influence of the frequency offset between the local oscillators at the transmitter and the receiver, otherwise the orthogonality between the sub-carriers will

be destroyed. If the sub-carriers are not orthogonal, they will cause ICI, and then the transmitted information will be difficult to reconstruct. Since the focus of this master's thesis report is channel estimation, it is assumed that the frequency offset estimation is ideal. [18]

As mentioned earlier, some kind of channel coding is usually used to reduce the bit error rate. However, the OFDM system still needs a frequency offset estimator and a channel estimator to achieve acceptable performance. A frequency offset estimator is needed to offset the influence of the frequency offset between the local oscillators at the transmitter and the receiver, otherwise the orthogonality between the sub-carriers will be destroyed. If the sub-carriers are not orthogonal, they will cause ICI, and then the transmitted information will be difficult to reconstruct, it is assumed that the frequency offset estimation is ideal. In the case of channel estimation, it is mainly done in the frequency dimension, that is, after OFDM signal demodulation. Since there is no ISI, each subcarrier is only affected by the multiplicative complex-valued scalar in the frequency domain, which will be estimated. These scalars are channel dependent and may vary over time and on different subcarriers.

The most preferred and commonly used method for estimating channel and frequency offset is to use pilot symbols. The pilot symbol is a symbol that the transmitter and receiver know in advance. The basic idea of the pilot symbol is that there is a strong correlation between the fading of the pilot symbol and the fading of the information data symbol sent close to the pilot symbol on time and subcarriers. [18]

Pilot symbols and information data symbols are usually placed on different sub-carriers in a certain pattern and elapsed over time, as shown in Figure 2.32.

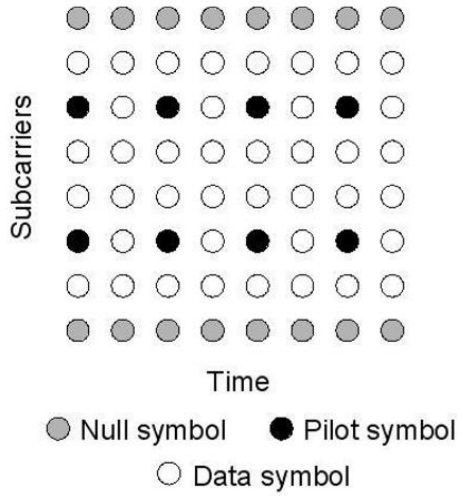

Figure2. 32: Example of OFDM signal pattern.

A new definition is also provided in Figure 2.32, namely the empty symbol. Null symbols are usually sent on empty subcarriers, which are just subcarriers without any transmission, hence the name. Some OFDM communication systems may have empty subcarriers at low subcarriers and high subcarriers to act as protection so that the OFDM communication system does not interfere with the communication of other devices with close frequencies. There are also some frequencies that are not used because they are used at the cell edge of other users in other cells. The vertical line in Figure 2.32 corresponds to one OFDM symbol, and there are eight OFDM symbols in the example figure. [18]

a. Modulation:

By using the Discrete Fourier Transform (DFT) and its corresponding Inverse Discrete Fourier Transform (IDFT), the ideas behind the analog implementation of OFDM can be extended to the digital domain. These mathematical operations are widely used to convert data between the time domain and the frequency domain. From an OFDM perspective, these transforms are interesting because they can be viewed as mapping data into orthogonal subcarriers. For example, IDFT is used to receive frequency domain data and convert it to time domain data. In order to perform this operation, IDFT will correlates the frequency domain input data and its orthogonal basis functions are sine

waves at certain frequencies. This correlation is equivalent to mapping the input data to a sine basis function.

In practice, OFDM systems are implemented using a combination of Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) blocks, which are mathematically equivalent versions of DFT and IDFT, respectively, but are more efficient to implement.

For example, n represents the frequency component index, S(n)denotes the original signal on the transmitter side. And the IFFT of the signal S(n) is [23]:

$$s(k) = \frac{1}{N}\sum_{n=0}^{N-1} S(n)e^{j2\pi nk/N}, k = 0, \dots N-1 \qquad (2.14)$$

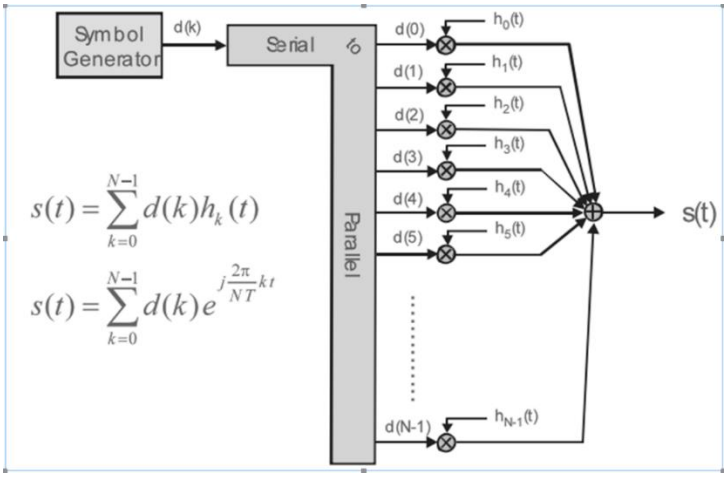

Figure2. 33: OFDM modulator.

Where N represents the number of frequency components, and s(k) is the resulting sampled signal, which is formed by the sum of the modulated frequency components S(n). Retrieve the digital frequency again where N represents the number of frequency components, and s(k) is the resulting sampled signal, which is formed by the sum of the modulation frequency components S(n). Retrieving the inverse equation of the digital frequency is [19]:

$$S(n) = \sum_{K=0}^{N-1} S(k)e^{-j2\pi nk/N} \qquad (2.15)$$

K=0, …N-1

Which corresponds to the N-point FFT of S(n).

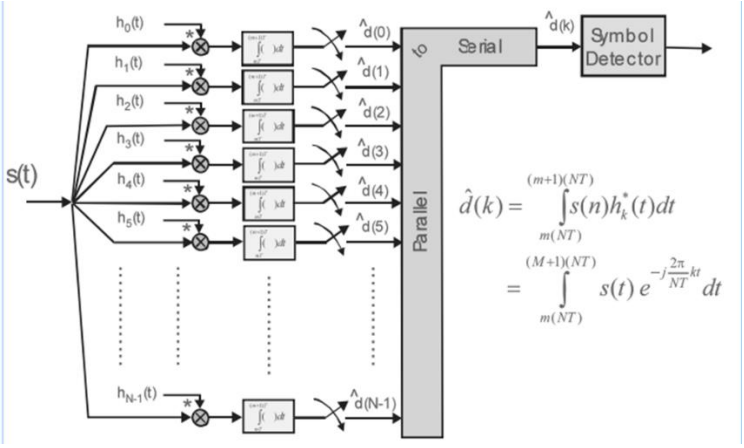

Figure2. 34:OFDM demodulator.

5. Conclution:

We can not speak of telecommunications and not speak of communication chains and modulations, in this chapter we have heviewed all types of modulations, we have presented the definitions and techniques, thier basic uses also the flaws that we have to overcome in every operation of receiving transmission (like fading, distortion etc).

CHAPITRE III

Implementation of the data link via the USRP type 2920 platform

1. Introduction:

In this chapter we will present the realization of modulation (FM, QPSK and 16QAM) by MATLAB software using the USRP 2029 card, and we will detail everything related to the processing and filtering blocks in the MATLAB transmit and receive schemes of each modulation.

The list below are the main hardware and software which are used in the following three experiments:

- **Hardware:**

_ Hp probook 450 laptop.
_ National instruments USRP-2920 – NI 50 MHz to 2.2 GHz.
_ Vert900 antenna.

- **Software:**

_ Windows XP.
_ Simulink (Matlab 2020).

2. NI 2920 USRPs installation:

To install NI USRP-2920, we have several steps to follow the basic steps:

- We must first install all the software we plan to use before installing the hardware, in our case we used MATLAB compatible software (Simulink).

- We configure the network (Ethernet only), so that the device can communicate with the host via Gigabit Ethernet.

- We are using a static IP address to configure the NI 2920 Host Ethernet Interface. The default IP address is 192.168.10.2 and 192.168.10.3. We need to configure a static IP address for the host Ethernet interface on the same subnet as the connected device to allow communication, as shown in the following table.

- We first install MATLAB on our PCs (2020 version).

Finally, we install USRP support from Communications Toolbox.

Component	**Address**
Host Ethernet interface static IP address	192.168.10.1
Host Ethernet interface subnet mask	255.255.255.0
Default NI USRP device IP address	192.168.10.2

Table2. 1:Static IP Addresses.

3. using MATLAB with USRP

MATLAB and Simulink connect to the USRP family of software-defined radios to provide a radio-in-the-loop environment for SISO and MIMO wireless system design, prototyping, and verification. Communications System Toolbox supports the USRP N200/N210, B200/B210, and X300/X310 SDRs to transmit and receive RF signals in real time, enabling the use of MATLAB and Simulink to configure radio parameters, generate waveforms, design algorithms, and measure and analyze signals. [20]

4. Implementation:

A. Simulating Real FM reception:

a. Description of the diagrams and parameters:

This model shows how to use the Universal Software Radio Peripheral (USR) device with Simulink to create an FM receiver.

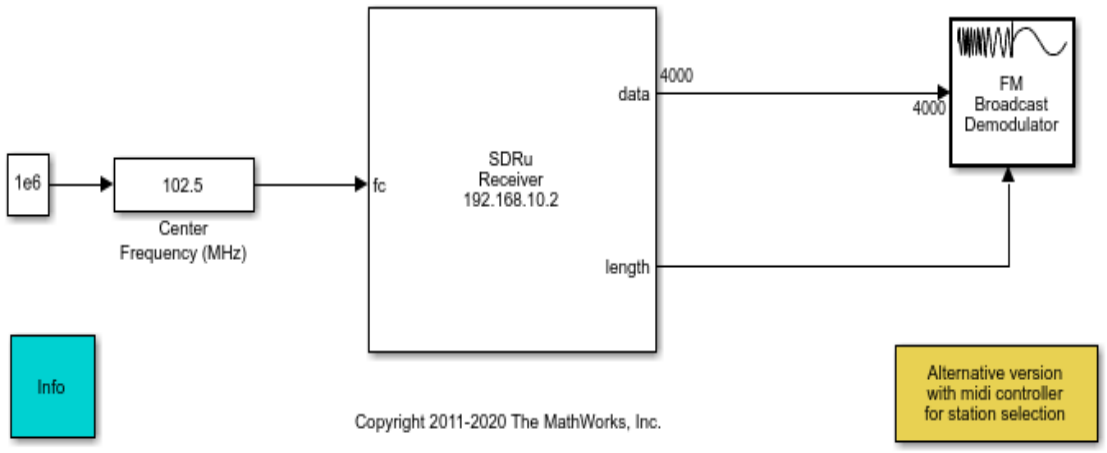

Figure3. 1:FM Broadcast Receiver with USRP (R) Hardware.

- **SDRu Receiver block:**

The SDRu Receiver block takes in the baseband discrete-time complex samples from the USRP hardware. The master clock rate and decimation factor are set to obtain sample rate of 200 kHz at the output of the SDRu Receiver block. For example, for a B210 radio, set Master Clock Rate to 20 MHz and Decimation Rate to 100. For N200, N210, and USRP2 radios master clock rate is fixed at 100 MHz.[21]

❖ **FM Broadcast Demodulator:**

The FM Broadcast Demodulator Baseband block converts the sampling rate of 240 kHz to 48 kHz, a native sampling rate for your host computer's audio device. According to the FM broadcast standard in the United States, the deemphasis lowpass filter time constant is set to 75 microseconds.[21]

b. Simulation process:

The process of this implementation is to receive the actual FM signal from the air by the USRP board and then it is processed in the FPGA and in the computer.

after demodulating the signal, we get a very high-quality FM signal, we can change station by changing frequencies on the center frequency block.

B. Simulating Real 16 QAM Transmission:

a. description of the diagrams and Parameters:

➢ part1:16-QAM transmitter with USRP(R) Hardware

In this section, we will explore the main components of the 16-QAM transmission block and detail the most important parameters.

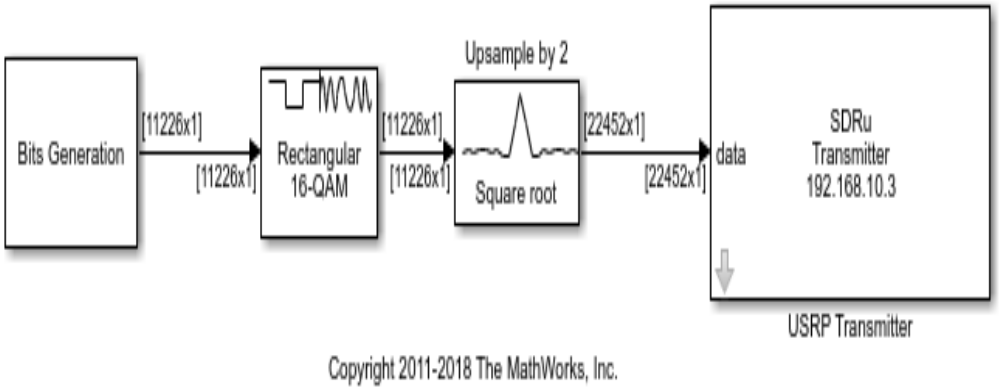

Figure3. 2: 16-QAM transmitter with USRP(R) Hardware

❖ Bits Generations:

Each data frame contains 26 bits header (For Sync Purpose) and 100 "Hello world ###" message. Scrambler is there to improve data transition density and frequency offset estimation. [1].

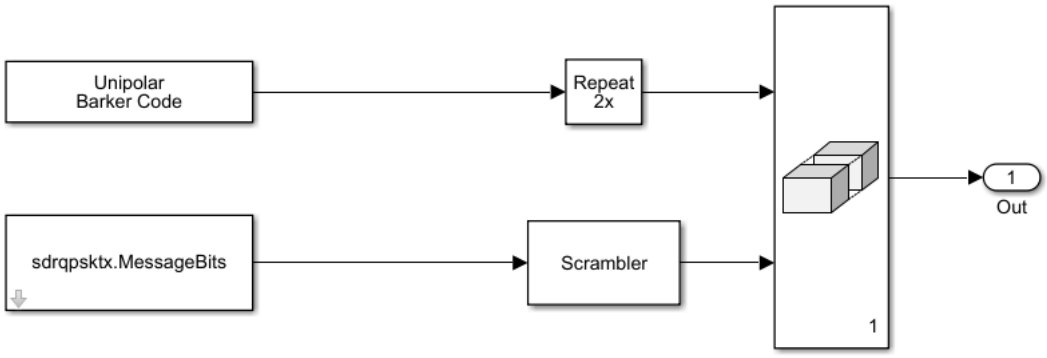

Figure3. 3: bits generations block

❖ Rectangular 16-QAM:

1)Description

The Rectangular QAM Modulator Baseband block modulates using M-ary quadrature amplitude modulation with a constellation on a rectangular lattice. The output is a baseband representation of the modulated signal. This block accepts a scalar or column vector input signal. [21].

2)Parameters:

M-ary number: The number of points in the signal constellation. It must have the form 2^K for some positive integer K.

Input type: Indicates whether the input consists of integers or groups of bits. [1].

Constellation ordering: Determines how the block maps each symbol to a group of output bits or integer [21].

Normalization method: Determines how the block scales the signal constellation. Choices are Min. distance between symbols, Average Power, and Peak Power. [21].

Minimum distance: The distance between two nearest constellation points. This field appears only when Normalization method is set to Min. distance between symbols. [1].

Phase offset (rad): The rotation of the signal constellation, in radians. [21].

Output data type: The output data type can be set to double, single, Fixed-point, User-defined, or inherit via back propagation. Setting this parameter to Fixed-point or User-defined enables fields in which you can further specify details. Setting this parameter to Inherit via back propagation, sets the output data type and scaling to match the following block. [21].

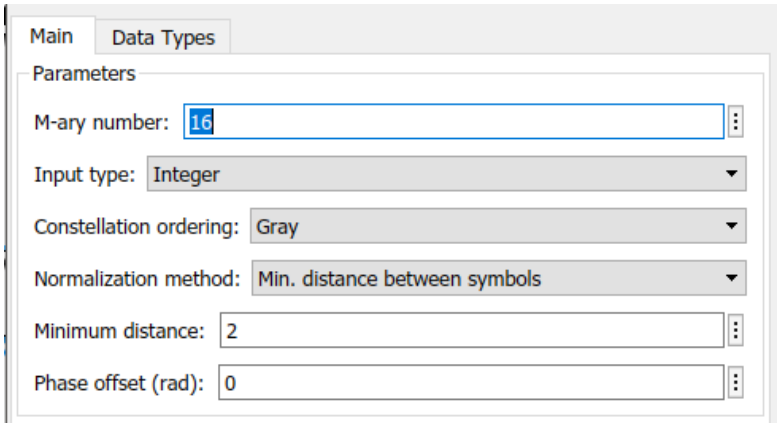

Figure3. 4: Parameter of Rectangular 16-QAM

- **Square root:**

The Raised Cosine Transmit Filter block up samples and filters the input signal using a normal raised cosine FIR filter or a square root raised cosine FIR filter. The block's icon shows the filter's impulse response. [21].

❖ SDRu Transmitter:

1)Description

The SDRu Transmitter block supports communication between Simulink and a Universal Software Radio Peripheral (USRP) device, enabling simulation and development for various software-defined radio applications. The SDRu Transmitter block and the USRP board must be on the same Ethernet subnetwork.

The SDRu Transmitter block accepts a column vector or matrix input signal from Simulink and transmits signal and control data to a USRP board using the Universal Hardware Driver (UHD) from Ettus Research. The SDRu Transmitter block is a Simulink sink that takes data from a model and sends it to a USRP board. The first call to this block can contain transient values, in this case the resulting packets contain undefined data.

This block diagram illustrates how Simulink, SDRu Transmitter and Receiver blocks, and USRP hardware interface. [21].

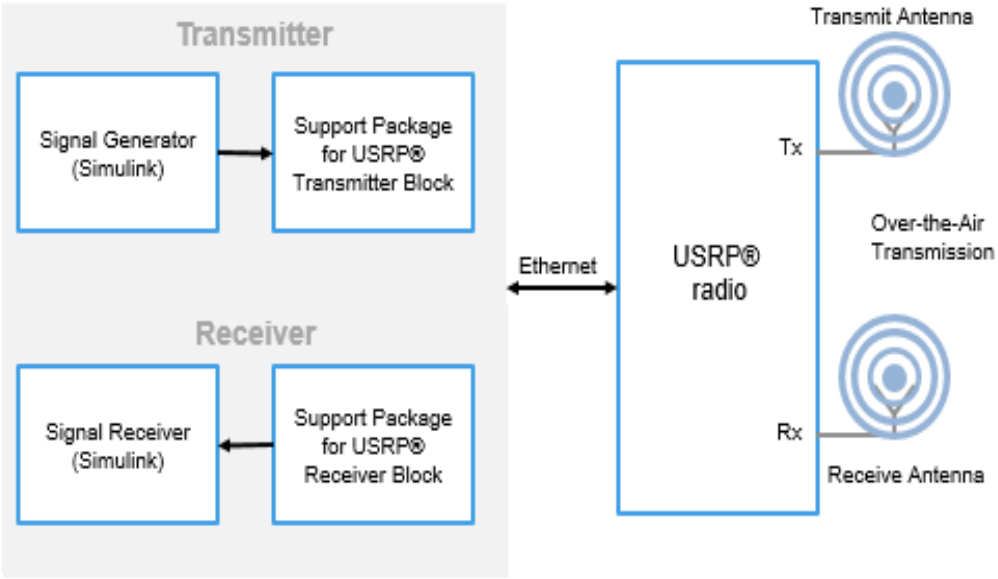

Figure3. 5: SDRu Transmitter-receiver blocks

2)Parameters:

IP address of the radio hardware, specified as a dotted quad expression. This parameter must match the physical IP address of the radio hardware assigned during hardware setup. If you configure the radio hardware with an IP address other than the default, update IP address accordingly. The IP address list displays IP addresses for USRP devices attached to the host computer. [21]

NOTE: More details on the parameters are shown in the receiver section.

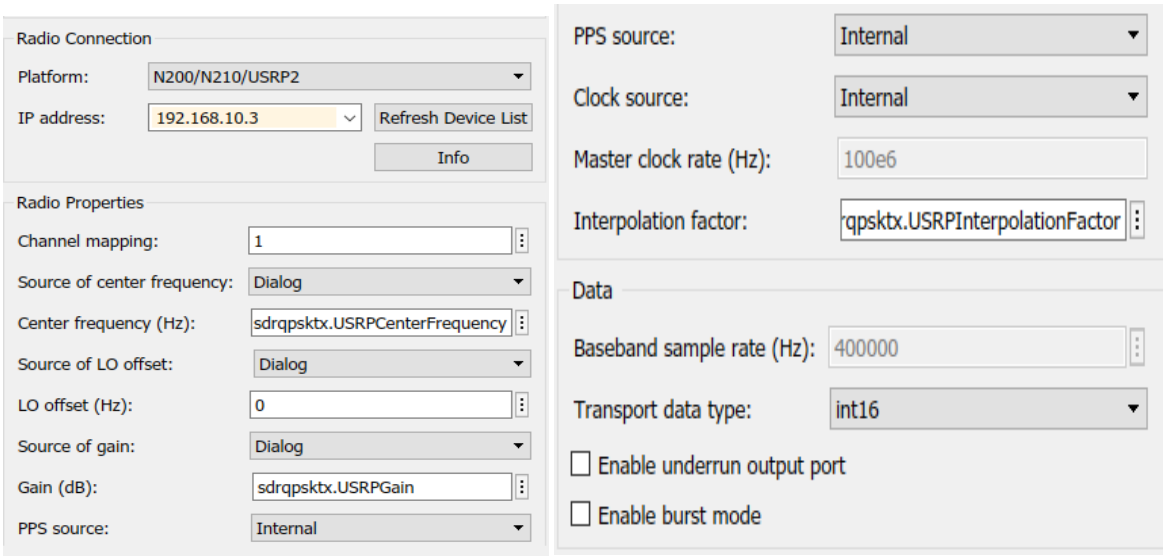

Figure3. 6: Parameter of sdru transmitter

➢ Part 2:16-QAM Receiver with USRP(R) Hardware

in this part we will discuss the reception block the same way we did with the transmission bloc (we detail the main components and parameters).

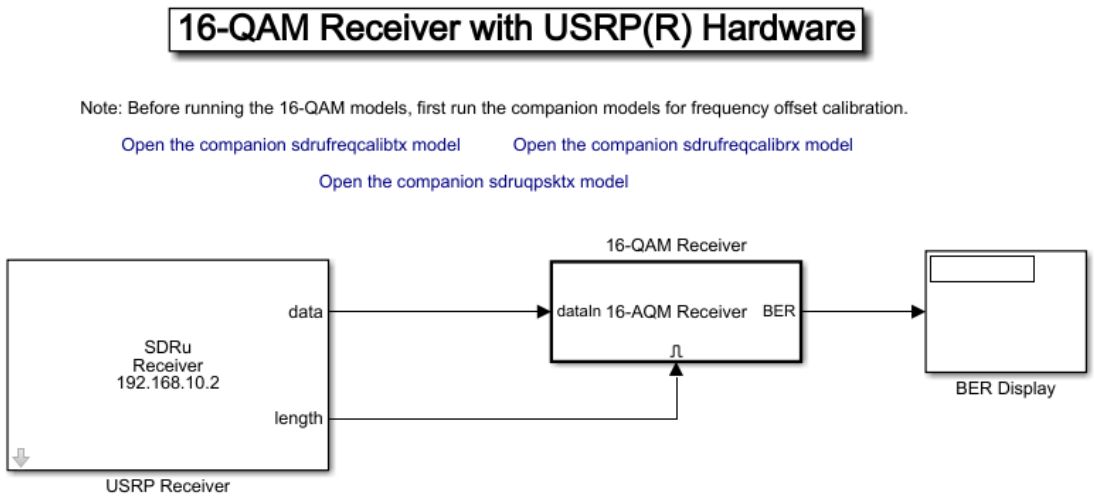

Figure3. 7: 16-QAM receiver withe USRP (R) hardware

❖ SDRu receiver:

1)Description

The SDRu Receiver block receives signal and control data from a USRP board using the Universal Hardware Driver (UHD) from Ettus Research. The SDRu Receiver block is a Simulink source that receives data from a USRP board and outputs a column vector or matrix signal with a fixed number of rows, when this block is called, it is possible that the host has not yet received any data from the USRP hardware. The data length port, length, indicates when valid data is present. When the data length port contains a zero value, there is no data. To qualify the execution of part of the model, use the data length with an enabled subsystem [21].

2)Parameters:

Platform — Radio to configure: Radio to configure, specified as one of USRP platforms listed [1].

IP address — IP address of radio hardware: 192.168.10.2 (default) IP address of the radio hardware.

This parameter must match the physical IP address of the radio hardware assigned during hardware setup. If you configure the radio hardware with an IP address other than the default, update IP address accordingly. The IP address list displays IP addresses for USRP devices attached to the host computer. To specify another known dotted quad IP address, enter it directly into this field. [21]

Channel mapping: specified as a positive integer scalar or vector [21].

Source of center frequency: specified as:

Dialog — Set the center frequency using the Center frequency (Hz) parameter.

Input port — Set the center frequency using the fc input port. [21].

Center frequency (Hz) — RF center frequency: RF center frequency in Hz, specified as a nonnegative finite scalar or vector of nonnegative finite scalars. The valid range of this parameter depends on the RF daughterboard of the USRP device. For a single channel (SISO), specify the value for the center frequency as a scalar. [21].

Gain (dB) — Receiver gain: Receiver gain in dB, specified as a scalar or vector. The valid gain range is from –4 dB to 71 dB and depends on the centre frequency. An incompatible gain and centre frequency combination return an error from the radio hardware. Set the value of gain based on the Channel Mapping configuration:

For a single channel (SISO), specify the gain as a scalar [21].

PPS source — Pulse per second (PPS) signal source Internal: specified as:

Internal — Uses the internal PPS signal of the USRP radio.

External — Uses the PPS signal from an external signal generator.

To synchronize the time for all channels of the bundled radios, provide a common external PPS signal to all the bundled radios and set PPS source to External [21].

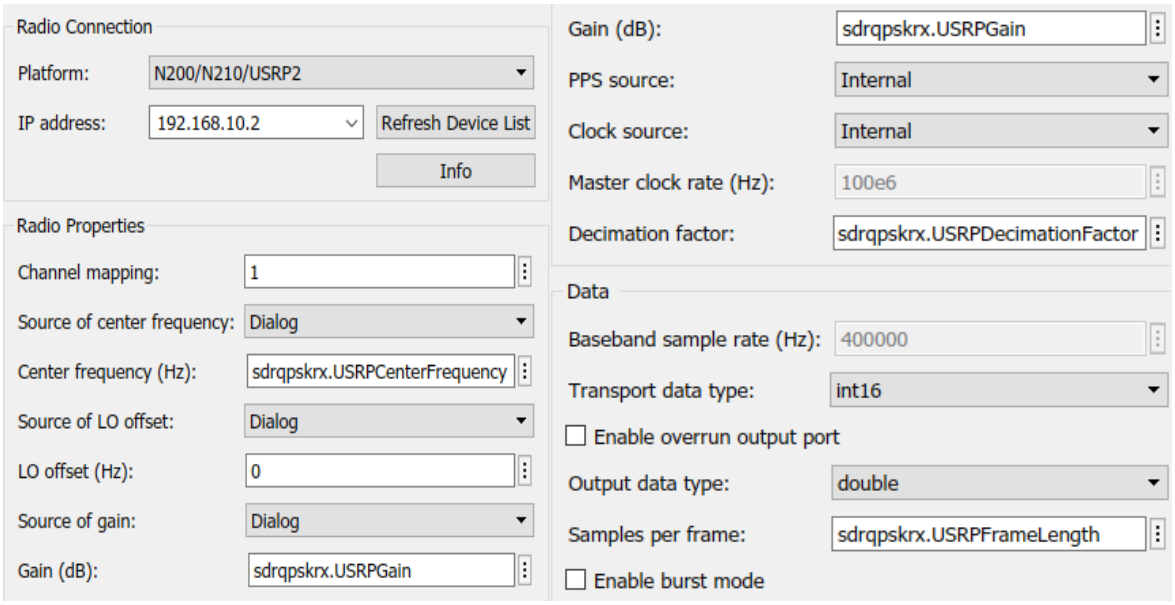

Figure3. 8: Parameter of SDR receiver

❖ BER Display:

1)Description:

The Display block shows the value of the input data. You can specify the frequency of the display. For numeric input data, you can also specify the format of display.

If the block input is an array, you can resize the block vertically or horizontally to show more than just the first element. If the block input is a vector, the block sequentially adds display fields from left to right and top to bottom. The block displays as many values as possible. A black triangle indicates that the block is not displaying all input array elements.

The Display block shows the first 200 elements of a vector signal and the first 20 rows and 10 columns of a matrix signal [21].

2)Parameters:

Figure3. 9: Parameter of BER display

❖ **16-QAM receiver:**

16- QAM receiver consists of several sub-blocs we will detail them in the following:

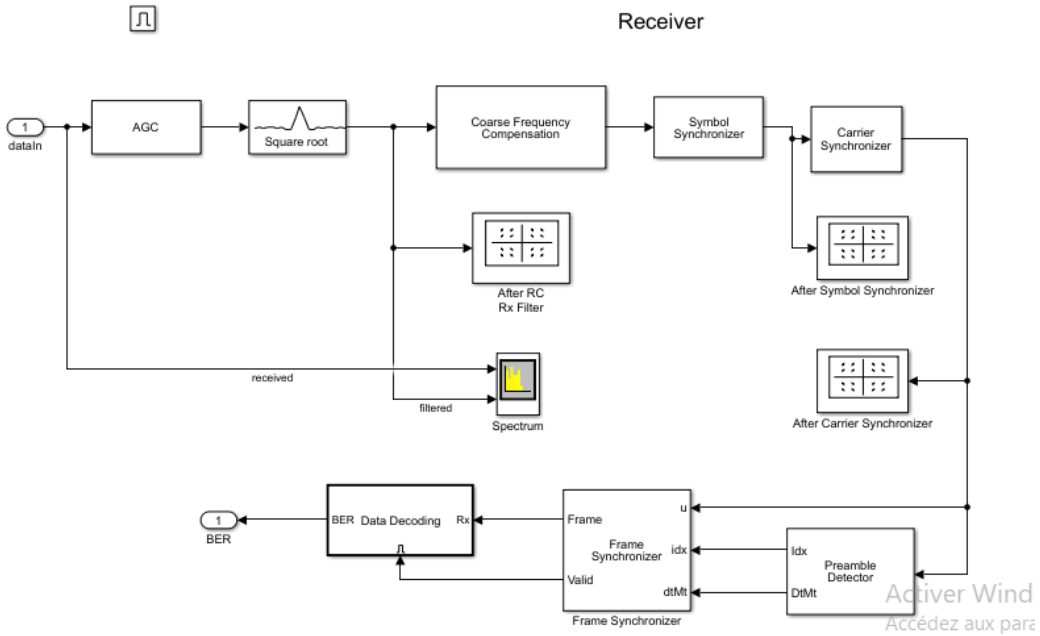

Figure3. 10: sdru receiver blocks

✓ **DataIn (InPort):**

1)Description:

Simulink software assigns Inport block port numbers according to these rules:

It automatically numbers the Inport blocks within a top-level system or subsystem sequentially, starting with 1.

If you add an Inport block, the label is the next available number.

If you delete an Inport block, other port numbers are automatically renumbered to ensure that the Inport blocks are in sequence and that no numbers are omitted [21].

If you copy an Inport block into a system, its port number is not renumbered unless its current number conflicts with an inport already in the system. If the copied Inport block port number is not in sequence, renumber the block. Otherwise, you get an error message when you run the simulation or update the block diagram. [21].

2)Parameters:

Port number — Position of port on parent block: Specify the order in which the port that corresponds to the block appears on the parent Subsystem or Model block.

_ If you add a block that creates another port, the port number is the next available number.

_ Deleting all blocks associated with a port deletes the port. Other ports are renumbered so that they are sequential and do not skip any numbers.

_ Specifying a port number that exceeds the number of ports creates a port for that number and for any skipped sequential numbers. [21].

Minimum — Minimum output value: Lower value of the output range that Simulink checks, this number must be a finite real double scalar value.

Maximum — Maximum output value

Upper value of the output range that Simulink checks, this number must be a finite real double scalar value. [1].

Data type — Output data type

Specify the output data type of the external input. The type can be inherited, specified directly, or expressed as a data type object such as Simulink.[21].

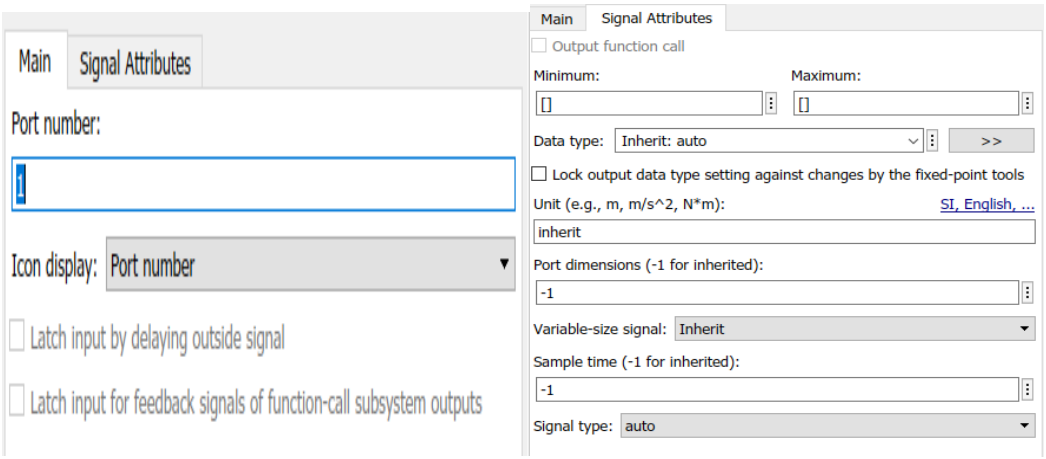

Figure3. 11: Parameters of DataIn.

- ✓ **AGC bloc:**

1)Description:

The automatic gain controller (AGC) block adaptively adjusts its gain to achieve a constant signal level at the output.[21].

2)Parameters:

Step size: Specify the step size for gain updates as a double-precision or single-precision real positive scalar. The default is 0.01, If you increase Step size, the AGC responds faster to changes in the input signal level. However, gain pumping also increases. [21].

Desired output power (W): Specify the desired output power level as a real positive scalar. The power level is specified in Watts referenced to 1 ohm. The default is 1. [21].

Averaging length: Specify the length of the averaging window in samples as a positive integer scalar. The default is 100. [21].

Maximum power gain (dB): Specify the maximum gain of the AGC in decibels as a positive scalar. The default is 60, If the AGC input signal power is very small, the AGC gain will be very large. This can cause problems when the input signal power suddenly increases. Use Maximum power gain (dB) to avoid this by limiting the gain that the AGC applies to the input signal. [21].

Enable output of estimated input power: Select this check box to provide an input signal power estimate to an output port, by default the check box is not selected. [21].

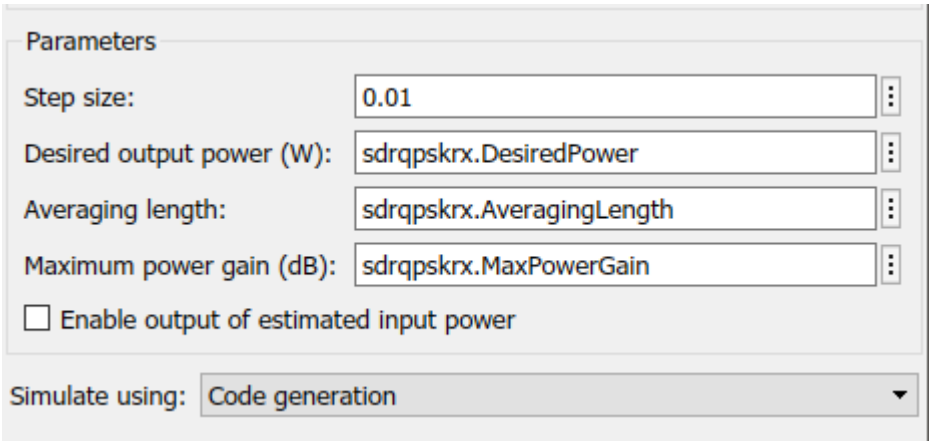

Figure3. 12: Parameter of AGC block

- ✓ **Square root:**

1)Description

The Raised Cosine Receive Filter block filters the input signal using a normal raised cosine FIR filter or a square root raised cosine FIR filter. It also down samples the filtered signal if you set the Output mode parameter to Down sampling. The FIR Decimation block implements this functionality. The Raised Cosine Receive Filter block's icon shows the filter's impulse response. [21].

2)Parameters:

Filter shape: Specify the filter shape as square root or Normal. [21].

Rolloff factor: Specify the roll off factor of the filter. Use a real number between 0 and 1. [1].

Filter span in symbols: Specify the number of symbols the filter spans as an even, integer-valued positive scalar. The default is 10. Because the ideal raised cosine filter has an infinite impulse response, the block truncates the impulse response to the number of symbols that this parameter specifies. [21].

Input samples per symbol: An integer greater than 1 representing the number of samples that represent one symbol in the input signal. [21].

Decimation factor: Specify the decimation factor the block applies to the input signal. The output samples per symbol equals the value of the input samples per symbol divided by the decimation factor. If the decimation factor is one, then the block only applies filtering. There is no decimation. [21].

Decimation offset: Specify the decimation offset in samples. Use a value between 0 and Decimation factor -1. [21].

Linear amplitude filter gain: Specify a positive scalar value that the block uses to scale the filter coefficients. By default, the block normalizes filter coefficients to provide unit energy gain. If you specify a gain other than 1, the block scales the normalized filter coefficients using the gain value you specify. [21].

Input processing: Specify how the block processes the input signal [21].

Coefficients: Choose how you specify the word length and the fraction length of the filter coefficients (numerator and/or denominator). [21].

Product output: Use this parameter to specify how you would like to designate the product output word and fraction lengths. [21].

Accumulator: Use this parameter to specify how you would like to designate the accumulator word and fraction lengths. [21].

Output: Choose how you specify the output word length and fraction length [21]

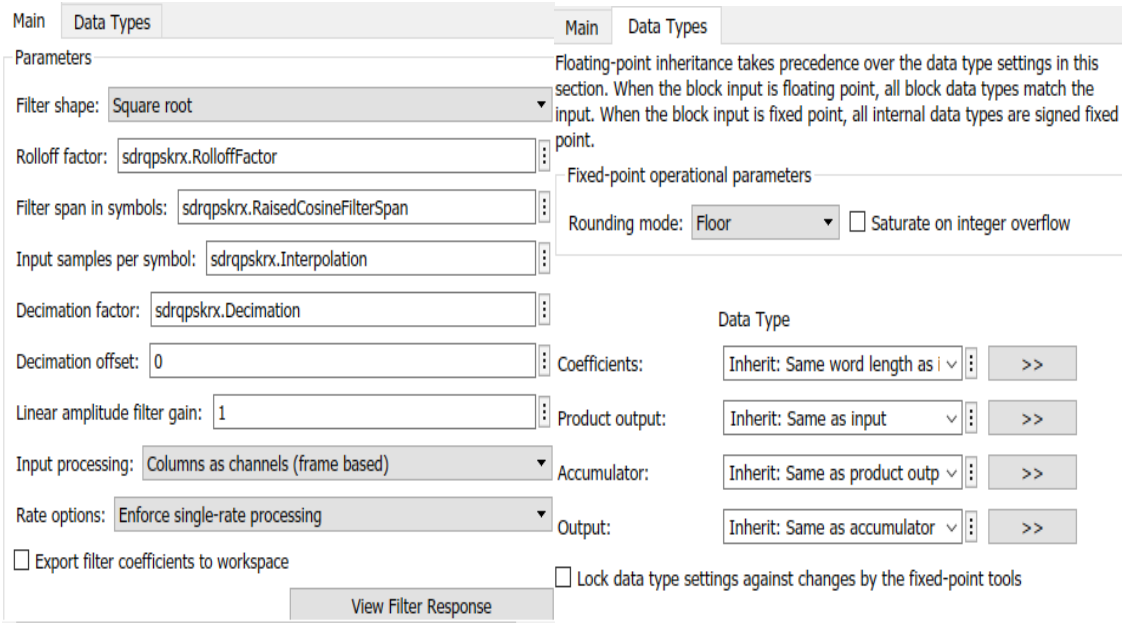

Figure3. 13: Parameter of Square root

✓ **Symbol Synchronizer:**

1)Description: The Symbol Synchronizer block corrects symbol timing clock skew for PAM, PSK, QAM, or OQPSK modulation schemes between a single-carrier transmitter and receiver. For more information [21].

2)Parameters:

Modulation type: Modulation type, specified as PAM/PSK/QAM, or OQPSK.

Timing error detector — Type of timing error detector: Type of timing error detector, specified as Zero-Crossing (decision-directed), Gardner (non-data-aided), Early-Late (non-data-aided), or Mueller-Muller (decision-directed), this parameter assigns the timing error detection scheme used in the synchronizer. [21].

Samples per symbol: Samples per symbol, specified as a positive integer greater than 1. [1].

Detector gain — Phase detector gain: Phase detector gain, specified as a positive scalar. [1].

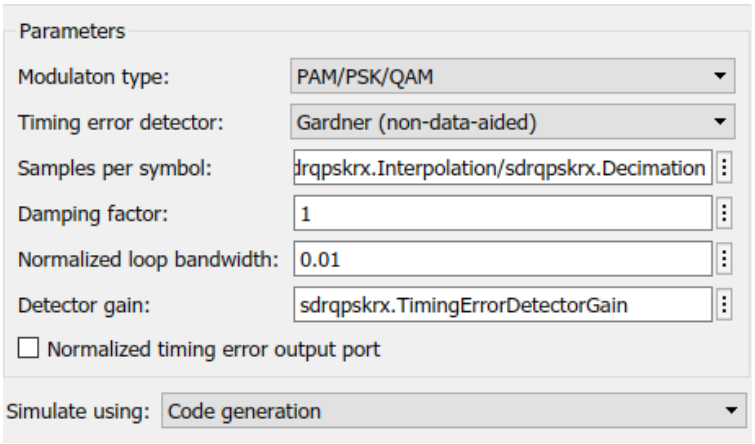

Figure3. 14: Parameter of samples per symbol

- ✓ **Carrier Synchronizer:**

1)Description

The Carrier Synchronizer block compensates for carrier frequency and phase offsets using a closed-loop approach for BPSK, QPSK, OQPSK, 8-PSK, QAM, and PAM modulation schemes. The block accepts a single input port. To obtain an estimate of the phase error in radians, select the Estimated phase error output port check box. The block accepts a sample- or frame-based complex input signal and returns a complex output signal and an a real phase estimate, the block outputs have the same dimensions as the input. [21].

2)Parameters

Modulation: Specify the modulation type as BPSK, QPSK, OQPSK, 8PSK, QAM, or PAM. [21].

Modulation phase offset: Specify the method used to calculate the modulation phase offset as either Auto or Custom. [21].

Samples per symbol: Specify the number of samples per symbol as a positive integer scalar. [21].

Damping factor: Specify the damping factor of the loop as a positive real finite scalar. [21].

Normalized loop bandwidth: Specify the normalized loop bandwidth as a real scalar between 0 and 1. The bandwidth is normalized by the sample rate of the carrier synchronizer block. [21].

Estimated phase error output port: Select this check box to provide the estimated phase error to an output port. [21].

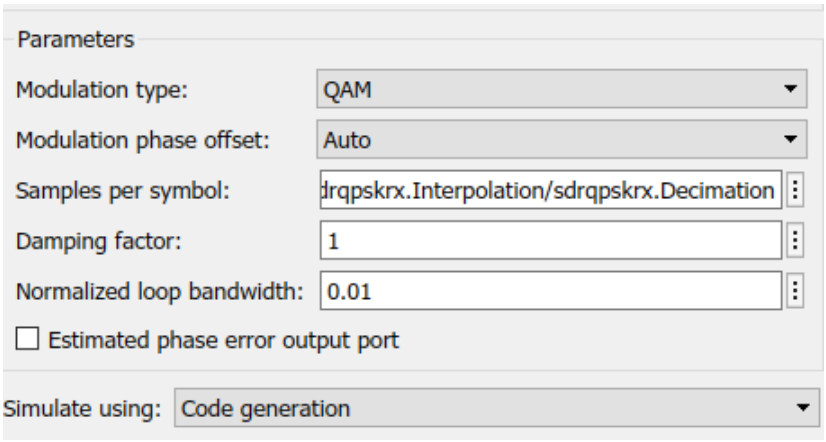

Figure3. 15: Parameter of Carrier Synchronizer

- ✓ **Constellation Diagram:**

1)Description

The Constellation Diagram block displays real and complex-valued floating and fixed-point signals in the I/Q plane. Use this block to perform qualitative and quantitative analysis on modulated single-carrier signals.

In the constellation diagram window, you can:

Input and plot multiple signals on a single constellation diagram. You can define one reference constellation for each input signal.

Choose which channels are displayed by selecting signals in the legend. Use the Show legend parameter to display the legend.

Display the EVM / MER Measurements panel, which displays calculated error vector magnitude (EVM) and modulation error ratio (MER) measurements. When a multichannel signal is input, use Trace Selection to choose the signal being measured. [21].

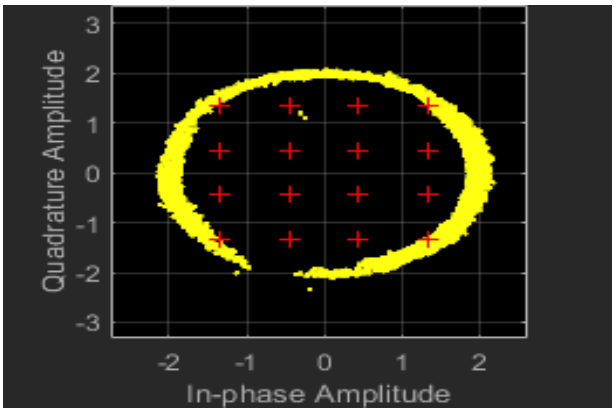

Figure3. 16: constellation diagram

b. simulation process :

in this section we will intreduce and analyze the implementation of 16-QAM Receiver and transmitter with USRP Hardwar.

The transmitter block generates and sends a modulated signal through the transmitting blocks and the transmitting antenna.

On the other hand, the receiving antenna picks up the signal and then it gets processed by the reception blocks (as explained above).

the sample rates of this simulation is 400 kHz.

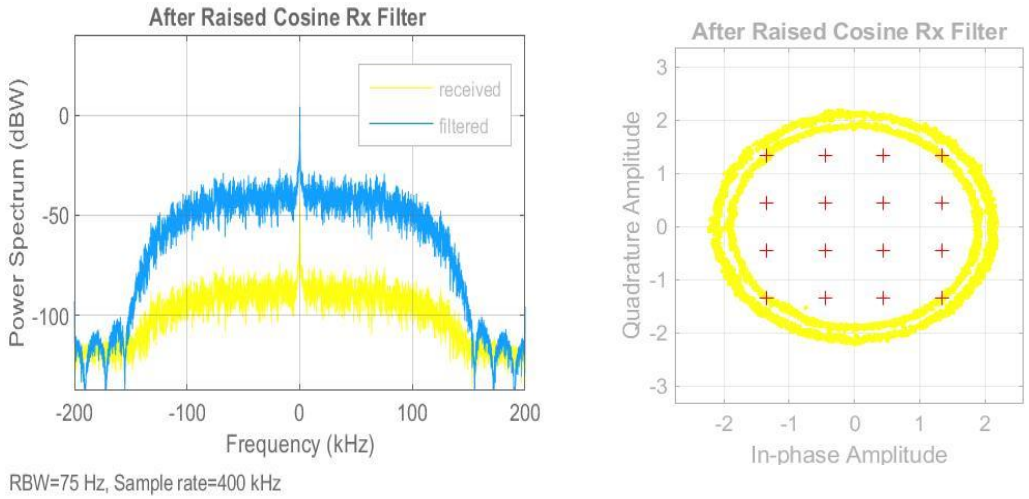

Figure3. 17: after raised cosine Rx filter

this lustration represents the comparison between the received signal and the filter, we can clearly see that they have almost the same graphical representations and it means that the final signal is more than perfect and the transmission via USRP is successful and that there are no losses or defects of signle.

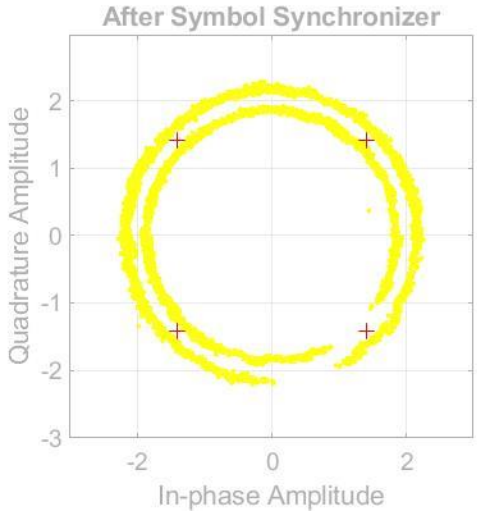

Figure3. 18: after symbol synchronizer

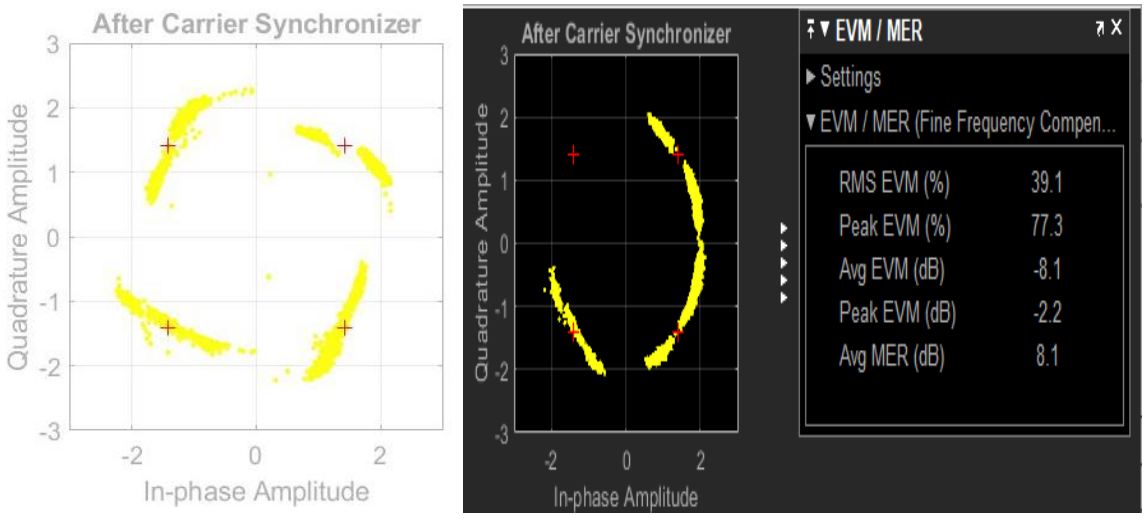

Figure3. 19: after carrier synchronizer

MER is a measure of the signal-to-noise ratio (SNR) in digital modulation applications. The module measures all outputs in dB.

The MER measurement module receives the received signal at the input port Rcv. It can use an ideal input signal at the reference port Ref, or optionally a reference constellation. The MER module then compares these inputs to output a measured value of modulation accuracy. The modulation error ratio is the ratio of the average reference signal power to the mean square error. This ratio corresponds to the SNR of the AWGN channel.

The module output always outputs MER in dB, and the minimum MER and X percentile MER values can be selected. The minimum MER represents the best-case MER value for each burst. For the X-percentile option, you can select the number of symbols processed in the output percentage calculation.

after all this we see that the single received is in good condition, there is no disturbance or noise

C. Simulating Real QPSK Transmission:

a. Description of the diagrams and Parameters:

- **part 1 : QPSK transmitter with USRP(R) Hardware:**

in this part we will simulate the transmission block based on QPSK modulation

NOTE: for more details see the section above (since we are always using the same blocks as the 16-QAM).

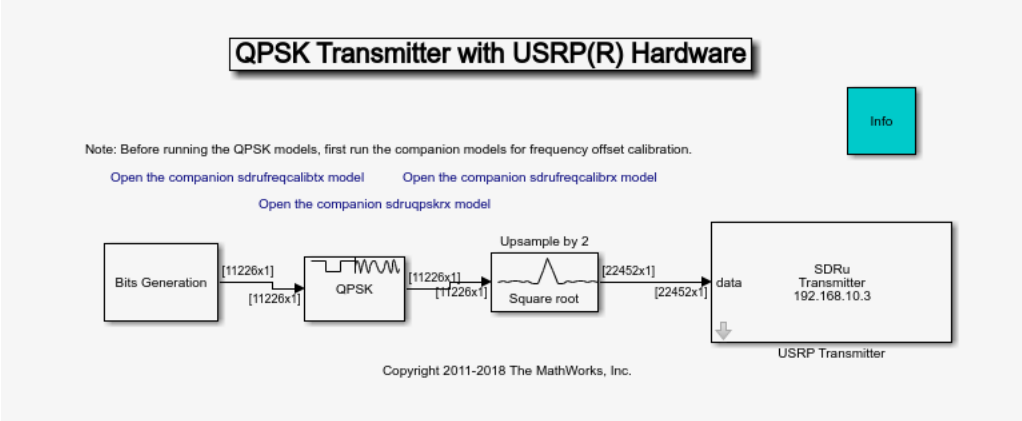

Figure3. 20: QPSK transmitter with USRP(R) hardware

- **<u>QPSK modulator:</u>**

1)Description

The QPSK Modulator Baseband block modulates using the quadrature phase shift keying method. The output is a baseband representation of the modulated signal.

Phase offset (rad)

The phase of the zeroth point of the signal constellation.

2)Parameters:

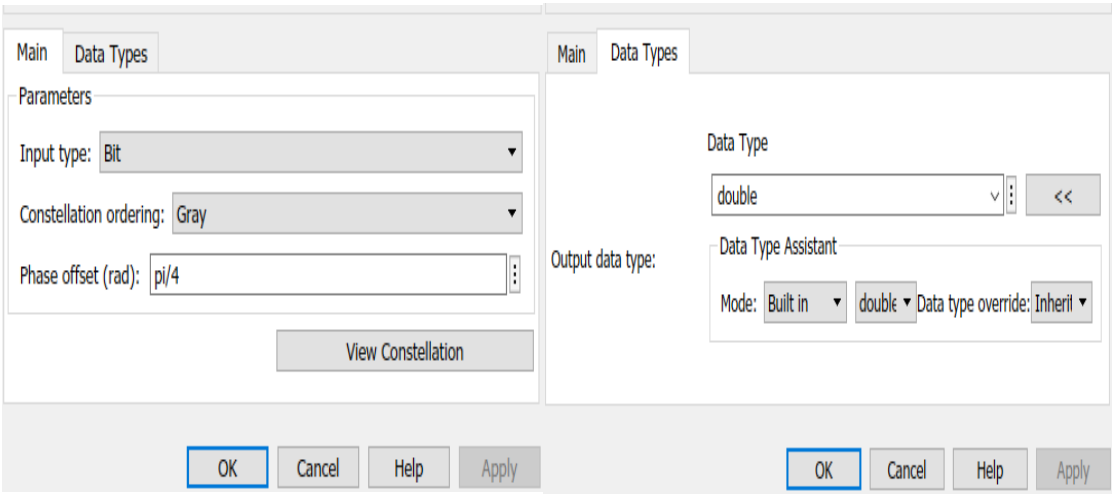

Figure3. 21: Parameter of QPSK modulator

➢ Part 2: QPSK receiver with USRP(R) Hardware:

➢

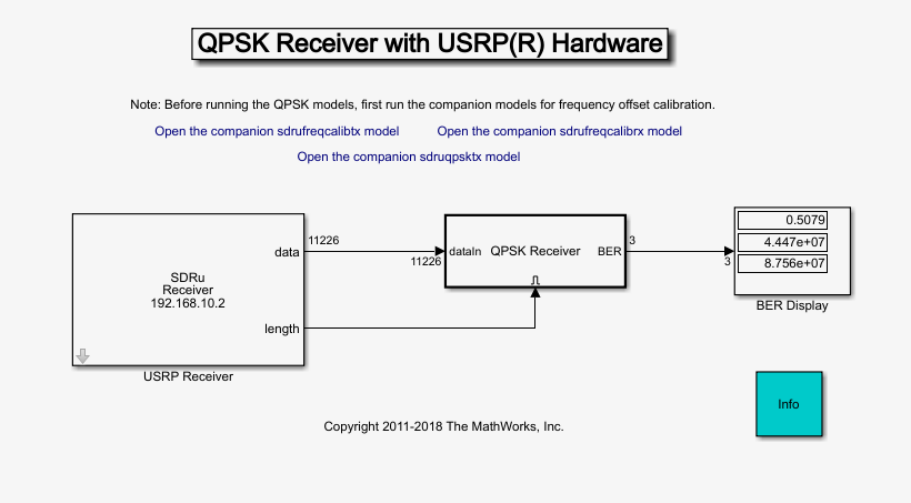

Figure3. 22: QPSK receiver with USRP(R) hardware

❖ QPSK Receiver:

We used the same blocks; the only difference is in the demodulation blocks (we changed the demodulation block of 16-QAM to a bpsk block).

The QPSK receiver consists of several sub-blocs we will also detail them in the following.

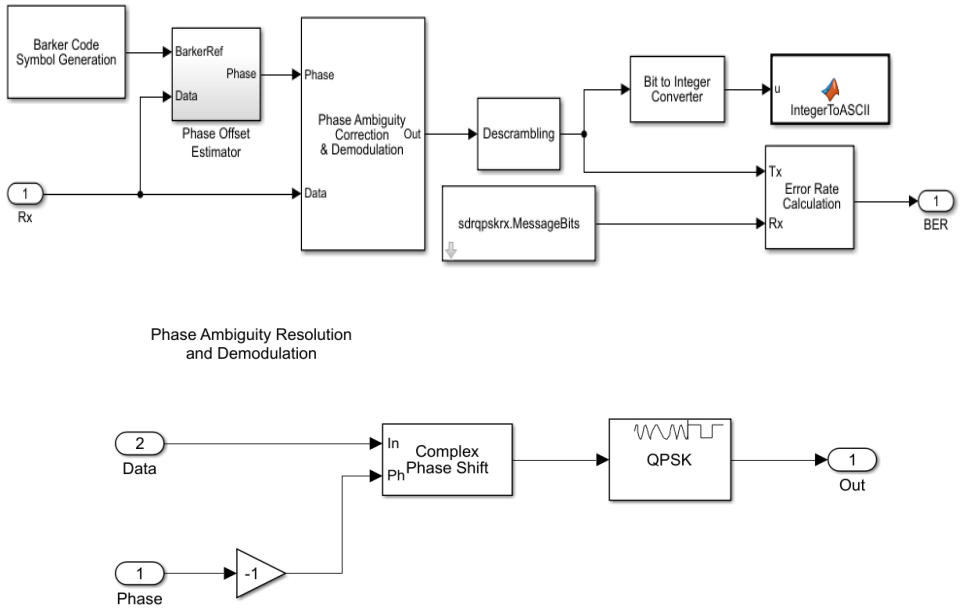

Figure3. 23: QPSK receiver

- ✓ **QPSK Demodulator Baseband:**

1)Description:

The QPSK Demodulator Baseband block demodulates a signal that was modulated using the quadrature phase shift keying method. The input is a baseband representation of the modulated signal.

2)Parameters:

Phase offset (rad): The phase of the zeroth point of the signal constellation.

Output type: Determines whether the output consists of integers or bits.

Decision type: Specifies the use of hard decision, LLR, or approximate LLR during demodulation. This parameter appears when you select Bit from the Output type drop-down list. The output values for Log-likelihood ratio and Approximate log-likelihood ratio decision types are of the same data type as the input values. For integer output, the block always performs Hard decision demodulation.

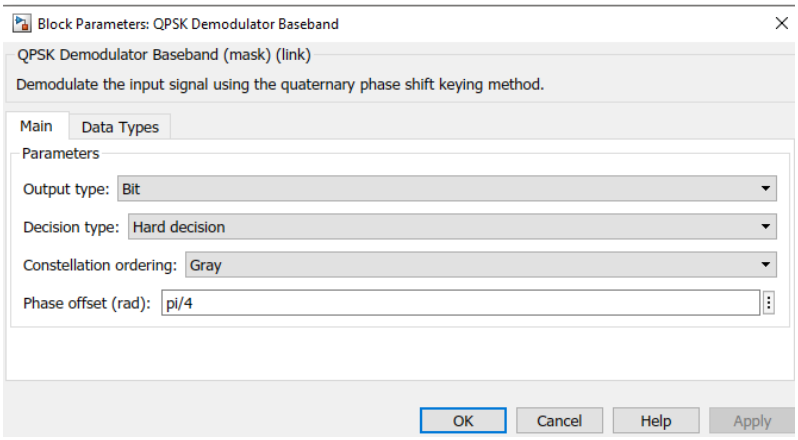

Figure3. 24: parameters of QPSK Demodulator Baseband

b. Simulation process:

in this section we will introduce and analyze the implementation of QPSK Receiver and transmitter with USRP Hardwar.

The transmitter block generates and sends a modulated signal through the transmitting blocks and the transmitting antenna.

On the other hand, the receiving antenna picks up the signal and then it gets processed by the reception blocks (as explained above).

the sample rates of this simulation is 400 kHz.

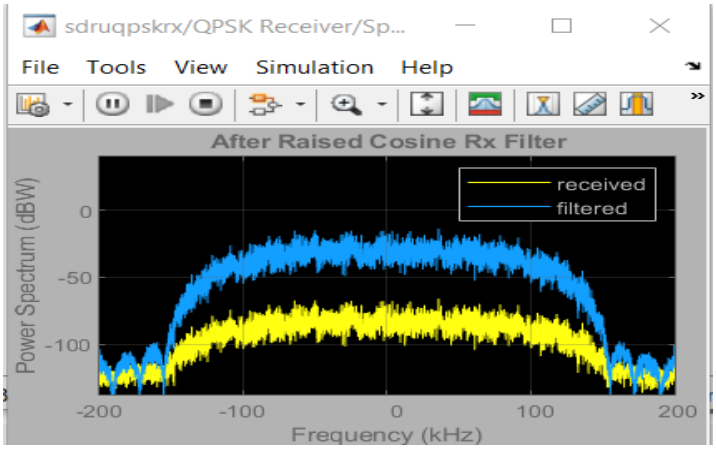

Figure3. 25: after Raised cosine Rx Filter

the filtered signal is in very good condition and it is a real proof that your transmission is very reliable and it is the same as with the 16-QAM modulation.

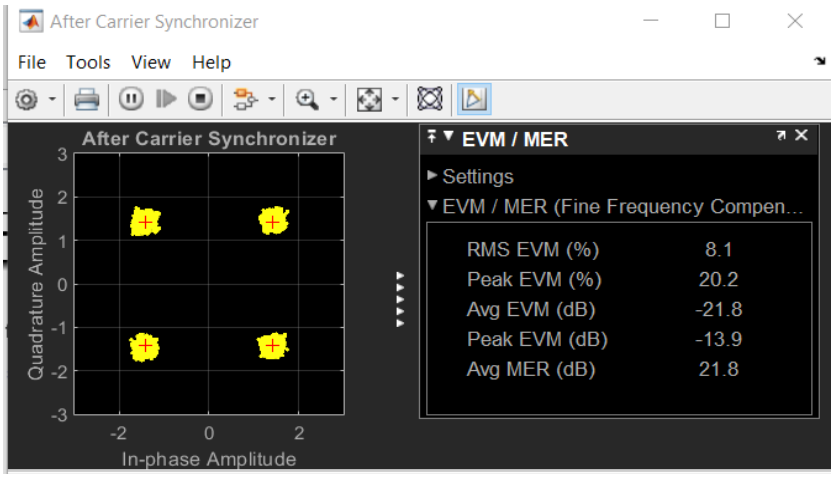

Figure3. 26: after carrier synchronizer

The single received is in good condition, there is no disturbance or noises, explained above (16-QAM) the synchronizer after carrier shows very good results also as proof of the reliability of this transmission.

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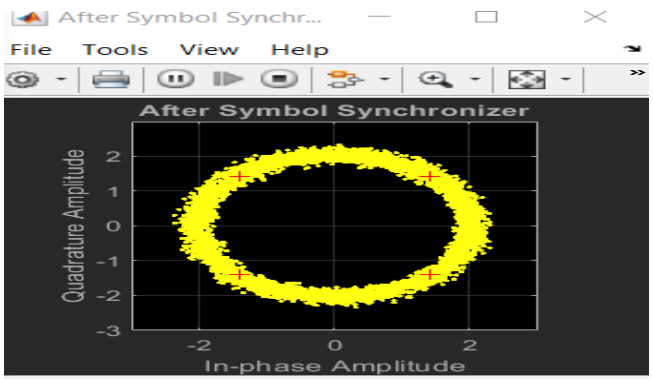

Figure3. 27: after symbol synchronizer

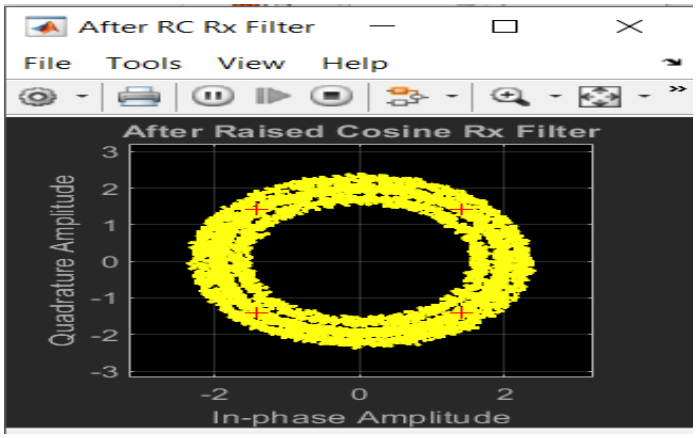

Figure3. 28: after raised cosine Rx filter

The Constellation Diagram block displays real and complex-valued floating and fixed-point signals in the I/Q plane. Use this block to perform qualitative and quantitative analysis on modulated single-carrier signals.

5. Conclusion:

we analyzed radio links based on modulations (FM, QPSK and 16-QAM) using the USRP 2920 platform as hardware and Simulink as software platform, we detailed each result starting with spectrum plots of each modulation and interpreted the signal shapes to the two transmission-reception processes.

after several tests, we saw how efficient and reliable the communication systems were.

General conclusion

Software-defined radios offer extensive advantages and features that have attracted researchers over the past few years. Because of their modularity, versatility, and digital nature, many new radio systems are being developed within software rather than hardware. Consisting of a versatile front-end hardware module, the signal processing of SDRs is often conducted within a general-purpose processor with a computer.

Many communication systems use Simulink to simulate theoretical systems and verify the functionality of the systems implemented. The ability to convert simulated systems into fully functional broadcast systems would add live testing capabilities to Simulink with minimal designer work.

it is possible to have such a capacity to transform a prototype into a real broadcasting thanks to USRP cards. The only hardware needed is the card itself with a powerful pocsse such as FPGA we can simulate an infinite number of transmission reception channels

after having passed moths with maps and the concept of USRP, we can say that the world is getting closer to a more future concept we no longer need to change the type or emplacement of components to improve transmissions.

the fusion between soft and hard is the solution, today we have an unlimited choice to create its own channel and a dozen of softwares to be done with it, such Simulink.

after some experiments and after dealing with real signal transmission with usrp cards, we managed to do real transmission reception with protaype and usrp only, after interpreting the result we saw the reliability and efficiency signal.

with few blocks on Simulink and effortlessly, we made three prototypes of an FM receiver and two ways real communication with two modulation types (16-QAM and QPSK).

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