

Low-Voltage/ Low-Power Integrated Circuits and Systems

LOW-VOLTAGE
MIXED-SIGNAL
CIRCUITS

EDITED BY
Edgar Sánchez-Sinencio
Andreas G. Andreou

Contents

Foreword	xix
Preface	xxi
Acknowledgments	xxiii
Contributors	xxv

Chapter 1	Introduction	1
	<i>Edgar Sánchez-Sinencio</i>	

1.1. Background	1
1.2. Overview of Book	2
References	5

Chapter 2	A Current-Based MOSFET Model for Integrated Circuit Design	7
	<i>Carlos Galup Montoro, Márcio Cherem Schneider, and Ana Isabela Araujo Cunha</i>	

2.1. Introduction	7
2.2. Fundamentals of the MOSFET Model	9
2.2.1. Basic Concepts and Definitions	9
2.2.2. Basic Approximations	10
2.2.3. Drain Current	13
2.2.4. Total Charges	16

2.2.5. Relationship between Inversion Charge Density and Terminal Voltages	17
2.3. Small-Signal MOSFET Model	21
2.3.1. Transconductances	22
2.3.2. Transconductance-to-Current Ratio	25
2.3.3. Intrinsic Capacitances	27
2.3.4. Extrinsic Element Modeling	31
2.3.5. Noise Model	32
2.3.6. Non-quasi-static Model	33
2.4. Second-Order Effects on MOSFET Characteristics	35
2.4.1. Charge Sharing and Drain-Induced Barrier Lowering	36
2.4.2. Mobility Reduction Due to Transversal Field	36
2.4.3. Velocity Saturation	37
2.4.4. Channel Length Modulation	38
2.4.5. Transconductance and Output Conductance	39
2.5. Application of the MOSFET Model to the Design of a Common-Source Amplifier	42
2.5.1. Design Equations	44
2.5.2. Common-Source Amplifier	45
2.5.3. Design Methodology	46
2.5.4. Simulation Results	47
2.6. Summary	48
Appendix A Determination of Q_S and Q_D	48
Appendix B Approximation of the Relationship between Current and Voltage	49
Appendix C Calculation of the Intrinsic Small-Signal Capacitances	49
Appendix D Discussion of the Non-quasi-static Model	52
References	53

Chapter 3 **A Review of the Performance of Available Integrated Circuit Components Under the Constraints of Low-Power Operation** 56

Derek F. Bowers

3.1. Introduction	56
3.2. What Exactly Is Low Power?	56
3.3. Semiconductor Choice	57
3.4. Active Devices	59
3.4.1. Bipolar Transistors	59
Low-Voltage Limitations of Conventional Bipolar Process	60
Low-Current Limitations of Conventional Bipolar Process	64
More Recent Bipolar Process Trends	67
3.4.2. MOSFETs	67
Low-Voltage Limitations of MOSFETs	68
Low-Current Limitations of MOSFETs	70
3.4.3. JFETs	72
3.5. Passive Devices	73

	3.5.1. Resistors	73
	3.5.2. Other Biasing Elements	75
	3.5.3. Capacitors	77
	3.5.4. Inductors	79
	3.6. Bandwidth and Noise Considerations	79
	3.6.1. Speed Restrictions at Low Voltages	79
	3.6.2. Speed Restrictions at Low Currents	80
	3.6.3. Noise Restrictions at Low Voltages	81
	3.6.4. <i>Noise Restrictions at Low Currents</i>	81
	Low-Current Noise in Bipolar Transistors	81
	Low-Current Noise in MOSFETs	82
	3.7. Conclusions	83
	References	83
Chapter 4	Exploiting Device Physics in Circuit Design for Efficient Computational Functions in Analog VLSI	85
	<i>Andreas G. Andreou</i>	
	4.1. Introduction	85
	4.1.1. From Device Physics to Analog VLSI Systems	86
	Device Level	87
	Circuit Level	89
	Architectural Level	90
	4.2. Technology and Devices	91
	4.2.1. Translinear Devices	95
	4.2.2. Floating-Gate MOS Transistor	98
	4.2.3. Large-Signal FGMOS Model	99
	4.3. Current-Mode Approach	101
	4.3.1. Current Conveyor	102
	4.4. Translinear Principle	104
	4.4.1. Translinear Loops	105
	Analysis of Translinear Circuits with MOS Transistors in Saturation	107
	Analysis of Circuits with MOS Transistors in Ohmic Regime	112
	4.4.2. Translinear Networks	113
	Translinear Spatial Averaging Networks	116
	4.4.3. General Result for MOS Translinear Loops	119
	4.4.4. Translinear Circuit Dynamics	120
	4.5. Contrast-Sensitive Silicon Retina	120
	4.6. Discussion	125
	Appendix A Bipolar Transistor Model	126
	References	128
Chapter 5	Low-Voltage Circuit Techniques Using Floating-Gate Transistors	133
	<i>Chong-Gun Yu and Randall L. Geiger</i>	
	5.1. Introduction	133

5.2. Concept of V_T Programming	135
5.2.1. Characteristics of Floating-Gate MOS Transistors	135
5.2.2. Methods of V_T Adjustment	137
5.2.3. A V_T Programming/Tuning Scheme	139
Threshold Voltage Tunable Circuit Structure	139
V_T Tuning Strategy	140
5.3. Performance Evaluation of Low-Voltage FGT Circuits	144
5.3.1. First-Order Scaling	146
5.3.2. Effects of Voltage Scaling in Analog Circuits	151
5.3.3. Effects of Voltage Scaling on Digital Circuits	156
5.4. Design Issues	160
5.4.1. V_T Extraction Schemes	161
Comparison of V_T Extraction Schemes	161
Principle of Matching-Free V_T Extractor	163
Model-Error Consideration	164
5.4.2. Limitations and Design Challenges	167
5.5. Conclusions	170
References	171
Chapter 6 Low-Power CMOS Digital Circuits	174
<i>Sherif H. K. Embabi</i>	
6.1. Introduction	174
6.2. Power and Energy Definitions	175
6.3. Power and Energy Consumption in Digital Circuits	175
6.3.1. Power Consumption in CMOS Digital Circuits	176
Static Power Dissipation	176
Dynamic Power Dissipation	176
6.3.2. Energy-Delay Product: A Metric for Low-Energy Design	177
6.4. Switching Activity in CMOS Digital Systems	178
6.5. Reduction of Energy in CMOS Digital Circuits	180
6.5.1. Power Supply Reduction	180
6.5.2. Switching Activity Reduction	184
Algorithmic Optimization	184
Architecture Optimization	185
Circuit Optimization	186
6.5.3. Reduction of Switching Capacitance	187
6.5.4. Reduction of Voltage Swing	189
6.6. Adiabatic Computing	193
Appendix A	196
Appendix B	201
References	204

Chapter 7	Low-Voltage Analog BiCMOS Circuit Building Blocks	207
	<i>Jaime Ramírez-Angulo</i>	
7.1.	Introduction	207
7.2.	Techniques to Reduce Voltage Supply Requirements	211
7.2.1.	Folding Techniques	212
7.2.2.	DC Level Shifting Techniques	213
7.2.3.	Floating-Gate Techniques	215
7.2.4.	MOS by Bipolar Replacement Techniques	216
7.2.5.	Subthreshold Techniques	217
7.2.6.	MOS Transistors Operating in Triode Mode	219
7.2.7.	Class AB Operation and Complementary Techniques	221
7.2.8.	Current-Mode Techniques	222
7.2.9.	Fully Differential Structures	225
7.2.10.	Flip-Over Techniques	227
7.3.	Examples of Low-Voltage BiCMOS Subsystems	228
7.3.1.	Programmable FIR and IIR Analog Filters	228
7.3.2.	Current-Mode Continuous-Time Filter and Oscillators	229
7.3.3.	Wide-Range Gain-Programmable OTA with Constant Bandwidth and Input Range	230
7.3.4.	Programmable Current-Mode Piecewise Linear Approximation	232
7.3.5.	Low-Voltage Operational Transconductance Amplifiers Using Multiple-Input Floating-Gate Transistors	234
7.4.	Conclusions	236
	References	237

Chapter 8	Low-Voltage CMOS Operational Amplifiers	242
	<i>Roelof F. Wassenaar, Sander L. J. Gierkink, Remco J. Wiegerink, and Jacob H. Botma</i>	
8.1.	Introduction	242
8.2.	Rail-to-Rail Constant- g_m Input Stages	243
8.2.1.	Rail-to-Rail Constant- g_m Input Stages Operating in the Weak-Inversion Domain	245
	Rail-to-Rail Constant- g_m Input Stage Using a Simple Current Mirror	245
	Rail-to-Rail Constant- g_m Input Stage Using Improved Wilson Current Mirrors	246
	Simple Rail-to-Rail Constant- g_m Input Stage Using a Minimum-Current Circuit	247
8.2.2.	Rail-to-Rail Constant- g_m Input Stages Operating in the Strong Inversion Domain	250
8.3.	Low-Voltage Rail-to-Rail CMOS Output Stages	256
8.3.1.	Low-Voltage Rail-to-Rail Output Stage with Feedback Class AB Control	259
8.3.2.	Low-Voltage Rail-to-Rail Class AB Output Stage without Local Feedback	263
8.4.	Complete Rail-to-Rail Input and Output Operational Amplifier	266

8.5. Conclusion	269
Acknowledgments	270
References	270

Chapter 9 **Low-Voltage/Low-Power Amplifiers with Optimized Dynamic Range and Bandwidth 272**

*Johan H. Huijsing, Klaas-Jan de Langen,
Ron Hogervorst, and Rudy G. H. Eschauzier*

9.1. Introduction	272
9.2. Dynamic Range—Supply Power Ratio	273
9.3. Voltage-Efficient Input Stages	278
9.4. Voltage- and Current-Efficient Output Stages	282
9.5. Bandwidth—Supply Power Ratio	287
9.6. Gain	290
9.7. Conclusions	298
Acknowledgments	299
References	299

Chapter 10 **Low-Voltage Analog CMOS Filter Design 301**

Michel Steyaert, J. Crols, and S. Gogaert

10.1. Introduction	301
10.2. Implications of Low-Power-Supply Voltages on Techniques for Analog CMOS Filters	302
10.3. Low-Voltage OTA-C Techniques	303
10.3.1. Introduction	303
10.3.2. Very Low Distortion Fully Differential OTA	303
Limitations of Easy Structures	303
Source-Degenerated Topologies	303
10.3.3. Low-Distortion Approach for Common-Mode Loop	305
Performance of a Practical Realized Structure	306
10.3.4. On-Chip Automatic Frequency Tuning	308
Drawbacks of Commonly Used Solutions	308
Automatic Frequency Tuning Technique Based on Charge Comparison	308
10.3.5. Conclusions	310
10.4. Very-Low-Voltage SC Techniques	311
10.4.1. Introduction	311
10.4.2. Limitations of SC at Low and Very Low Voltages	311
10.4.3. Switched Capacitor at Very Low Voltages	315
Use of a Dedicated Low- V_T Process	315
Clock Signal Voltage Multiplication	315
Switched-Opamp Technique	318
10.4.4. Conclusions	324
References	325

Chapter 11 Continuous-Time Low-Voltage Current-Mode Filters 327
Edgar Sánchez-Sinencio and Sterling L. Smith

- 11.1. Introduction 327
- 11.2. Basic Building Blocks 328
 - 11.2.1. High-Frequency Parasitic Effects 340
 - 11.2.2. Large-Signal Operation 343
 - 11.2.3. Effects of Transistor Mismatch on Distortion 344
 - 11.2.4. Phase Compensation Techniques 344
- 11.3. Biquadratic Current-Mode Filters 346
 - 11.3.1. Biquadratic Architecture Nonidealities 352
- 11.4. CMOS Experimental Results: Example 353
 - References 356

Chapter 12 High-Efficiency Low-Voltage DC-DC Conversion for Portable Applications 361

*Anthony J. Stratakos, Charles R. Sullivan,
 Seth R. Sanders, and Robert W. Brodersen*

- 12.1. Introduction 361
- 12.2. Pulse-Width-Modulated DC-DC Converter 362
 - 12.2.1. Buck Converter 362
 - Output Filter Design 363
 - Buck Converter Efficiency 365
- 12.3. Converter Miniaturization 366
 - 12.3.1. High-Frequency Operation 367
 - 12.3.2. High Current Ripple 368
 - 12.3.3. High Integration 369
- 12.4. Circuit Techniques for High Efficiency 369
 - 12.4.1. Synchronous Rectification 369
 - Synchronous Rectifier Control 370
 - 12.4.2. Zero-Voltage Switching 370
 - Design of a ZVS Buck Circuit 372
 - 12.4.3. Adaptive Dead-Time Control 372
 - 12.4.4. Power Transistor Sizing 375
 - 12.4.5. Reduced-Swing Gate-Drive 376
 - V_g Selection 381
 - Reduced Gate-Swing Circuit Implementation 383
 - 12.4.6. PWM-PFM Control for Improved Light-Load Efficiency 384
- 12.5. Example Design 385
- 12.6. Physical Design Considerations 387
 - 12.6.1. Power Transistor Layout 387
 - 12.6.2. Board-Level Assembly 388
 - 12.6.3. Magnetic Components 389
 - Magnetic Cores 390
- 12.7. Alternatives to Switching Regulators 391
 - 12.7.1. Linear Regulators 391
 - 12.7.2. Switched-Capacitor Converters 392

12.8. Conclusion	395
References	395

Chapter 13 **Two New Directions in Low-Power Digital CMOS VLSI Design** 398

Vitit Kantabutra

13.1. Introduction	398
13.2. State Assignment Approach to Low-Power Asynchronous CMOS Circuit Design	399
13.2.1. Introduction	399
13.2.2. Background and Motivation	400
13.2.3. General, Race-Free State Assignment Algorithm	402
States of State Transition Diagram	404
Naming the Copies	405
Numbering the States	405
Modifying Numbering of States in C_ϕ	405
Modifying Numbering of States in Each Primary Copy $C_{\{j\}}$	405
Modifying Numbering of States in Each Secondary Copy $C_{\{j_1, j_2, \dots, j_n\}}$	405
Replacing Bad Transitions by Good Ones	405
Choosing Destination State	406
Correctness of Algorithm	406
13.2.4. Comparison between Race-Free Circuits and Circuits with Races: Experiment Using Circuit-Level Simulation	406
13.2.5. Simulation Results and Discussion	409
13.3. Using Complex Gates in Low-Power CMOS Design	413
13.3.1. Introduction	413
13.3.2. Method of Study	414
The Circuits	415
Testing the Circuits	422
Statistical Analysis	424
13.4. Conclusions and Further Discussions	428
Acknowledgments	429
References	429

Chapter 14 **Low-Power CMOS Data Conversion** 432

Marcel J. M. Pelgrom

14.1. Introduction	432
14.1.1. Analog-to-Digital Conversion: Basic Terminology	433
14.2. System	435
14.2.1. Specification of Functionality	436
Power Shifts	438
14.2.2. Signal-Processing Strategy	439
Sampling Rate and Bandwidth	439
Sample Rate and Accuracy	440

	Sampling of Modulated Signals	441
	14.2.3. Implementing System Functions	441
	Conversion of Modulated Signals	442
	Oversampled D/A Converter	443
14.3.	Integrated Circuit	444
	14.3.1. Technology	444
	Signal Swing	444
	Feature Size	445
	Process Options	446
	Tolerances	447
	14.3.2. Conversion Architectures	449
	D/A Converters	449
	A/D Converters	451
	Yield	454
	Noise	457
	Jitter	459
14.4.	Implementation	459
	14.4.1. Status of Data Converters	459
	14.4.2. CMOS Digital-to-Analog Converters	461
	Current-Domain D/A Conversion	461
	Resistor String D/A Converter	461
	A Comparison	466
	14.4.3. High-Speed Analog-to-Digital Converters	467
	The Comparator	467
	Full-Flash A/D Converter	469
	Successive-Approximation A/D Converter	469
	Multistep A/D Converter	471
	A Comparison	472
14.5.	Physical Restrictions	472
	14.5.1. Systematic and Random Offsets	472
	14.5.2. Component Matching	475
	Low Voltage and Matching	477
	Limits of Power and Accuracy	479
14.6.	Conclusion	482
	Acknowledgments	482
	References	482

Chapter 15 **Low-Power Multiplierless YUV-to-RGB Converter Based on Human Vision Perception** 485

*Teresa H. Meng, Benjamin M. Gordon,
and Navin Chaddha*

15.1.	Introduction	485
15.2.	Distortion Measure	486
15.3.	Coefficient Selection	487
15.4.	Architecture	490
15.5.	Low-Power Adder Design	491
	15.5.1. Low-Power Design Guidelines	491
	Scaling Factor in a Buffer Chain	492

Minimizing the Occurrence of Spurious Switching	492
Equalizing the Delays Between Logic Paths	492
15.5.2. Design Example: The Adder	494
15.6. Performance	497
15.7. Conclusions	499
References	499

Chapter 16 **Micropower Systems for Implantable Defibrillators and Pacemakers 500**

Marwan Jabri and Richard Coggins

16.1. Introduction	500
16.2. Energy Minimization Strategies for Digital Circuits	501
16.3. Brief Review of CMOS Subthreshold Operation	503
16.3.1. Characteristics	503
16.3.2. Advantages	503
16.3.3. Design Considerations	504
16.4. Pattern Recognition in ICTS	504
16.5. Analog Subthreshold Multilayer Perceptrons	506
16.5.1. Training Issues	506
16.5.2. Wattle	506
Architecture	507
Implementation	507
Performance Evaluation	508
16.5.3. Snake	511
Architecture	511
Implementation	511
Performance Evaluation	513
16.6. Discussion	515
16.6.1. Other Implementation Methods	516
Adiabatic Logic	516
Low-Threshold Systems	516
16.7. Conclusions	516
References	517

Chapter 17 **An Information Theoretic Framework for Comparing the Bit Energy of Signal Representations at the Circuit Level 519**

Andreas G. Andreou and Paul M. Furth

17.1. Introduction	519
17.2. A Communication Theory Model for VLSI	521
17.3. Information and Communication Theory Primer	522
17.3.1. Entropy and Mutual Information	523
17.3.2. Shannon Channel Capacity	524
17.4. Four Signal Representations: Physical Encodings	526
17.4.1. Continuous-Value, Continuous-Time Circuit	527
17.4.2. Continuous-Value, Discrete-Time Circuit	529
17.4.3. Discrete-Value, Discrete-Time Circuit	531

- 17.4.4. Discrete-Value, Continuous-time Circuit 534
- 17.5. Results 535
- 17.6. Discussion 537
- Appendix A 538
- References 540

Chapter 18 A Synchronous Gated-Clock Strategy for Low-Power Design of Telecom ASICs 541

Paul Vanoostende and Geert Van Wauwe

- 18.1. Introduction 541
- 18.2. Power Contributions: Importance 542
- 18.3. Synchronous Gated-Clock Strategy 544
 - 18.3.1. Obtaining Advantages of Fully Synchronous Design 544
 - 18.3.2. Derivation of Load Signal 545
 - XOR-Based Approach 545
 - Exploiting Conditional Assignments 546
- 18.4. Results 547
 - 18.4.1. Gated Clock Inside Library Modules 547
 - 18.4.2. Exploiting Conditional Expressions 548
 - Simple Example 548
 - Real-Life Example 549
- 18.5. Conclusions 550
- References 550

Index 551

About the Editors 561

The design of low-voltage, low-power devices is becoming a primary concern for many designers. The need for more efficient devices are becoming so important that many designers are now designing devices that are not only more efficient but also more powerful. And, of course, the need for more efficient devices is not limited to the design of new devices, but also to the design of existing devices. Many modern devices are still with us and are increasing in power consumption.

The design of low-voltage, low-power devices is becoming a primary concern for many designers. The need for more efficient devices are becoming so important that many designers are now designing devices that are not only more efficient but also more powerful. And, of course, the need for more efficient devices is not limited to the design of new devices, but also to the design of existing devices. Many modern devices are still with us and are increasing in power consumption.

The editors of this volume have assembled a distinguished group of contributors who address nearly every aspect of low-voltage and low-power design. They provide a snapshot of the state of the art in this exciting and rapidly changing area. Their contributions range from device technology to the practical design of low-power systems. The book includes a wealth of design examples, including the design of logic blocks, registers, logic gates, filters, and many other circuits.

This volume is an essential reference for engineers involved in the design of low-voltage and low-power devices and to researchers who want to stay up-to-date on the state of the art and the current problems that remain to be solved in the area of low-power electronics.

*Alan S. Sedra
Carolina, Colorado*